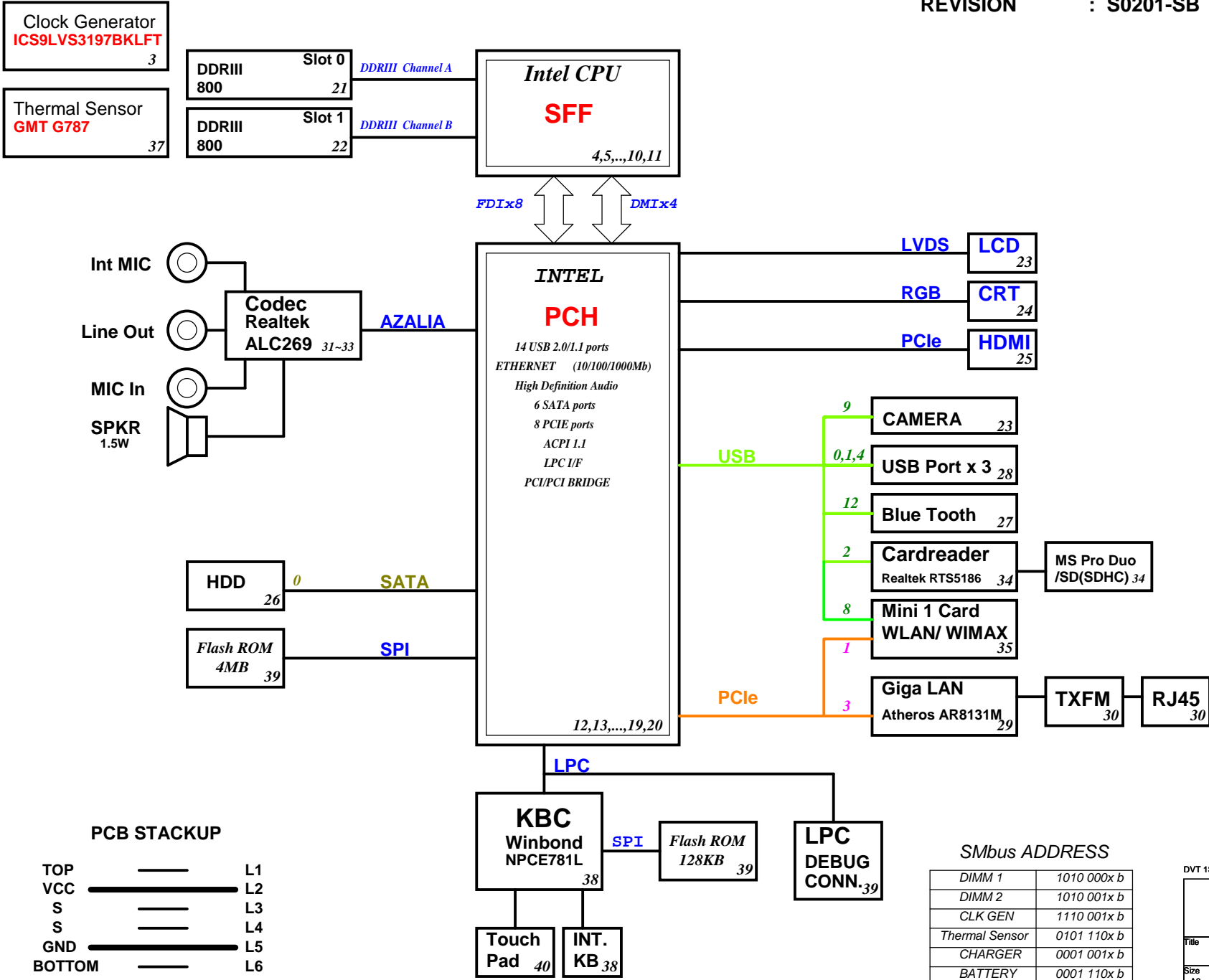


# TUCANA Block Diagram

PROJECT CODE : 91.4KK01.001  
PCB P/N : 48.4KK01.0SB  
REVISION : S0201-SB



SYSTEM DC/DC RT8223 47	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5
RT8209 49	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(20A)
RT8209 48	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(9.4A)
RT9026 51	
INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 1.2A
CHARGER BQ24751 52	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
CPU DC/DC ADP3211 46	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 27A
GFX Core ADP3211 50	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 11A

SMbus ADDRESS

DIMM 1	1010 000x b
DIMM 2	1010 001x b
CLK GEN	1110 001x b
Thermal Sensor	0101 110x b
CHARGER	0001 001x b
BATTERY	0001 110x b

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Title: BLOCK DIAGRAM

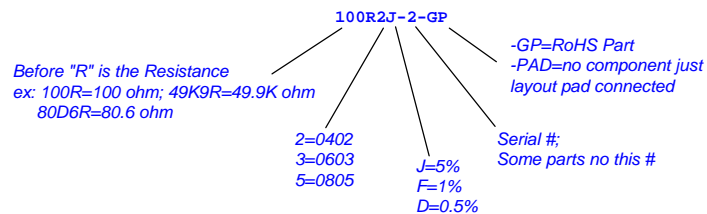
Size A3	Document Number	Rev SB
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Date: Wednesday, July 07, 2010 Sheet 1 of 56

## PCH Strapping

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> <b>Default Mode:</b> Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	<b>Default Mode:</b> Internal pull-up. <b>Low (0) = Top Block Swap Mode</b> (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	<b>High (1) = Integrated VRM is enabled</b> <b>Low (0) = Integrated VRM is disabled</b>
GNT0#, GNT1#	<b>Default (SPI):</b> Left both GNT0# and GNT1# floating. No pull up required. <b>Boot from PCI:</b> Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. <b>Boot from LPC:</b> Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	<b>Default - Internal pull-up.</b> <b>Low (0)=</b> Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	<b>Default:</b> Do not pull low. <b>Disable ME in Manufacturing Mode:</b> Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	<b>Enable iTPM:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable iTPM:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable Danbury:</b> Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	<b>Low (0):</b> Flash Descriptor Security will be overridden. <b>High (1) :</b> Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

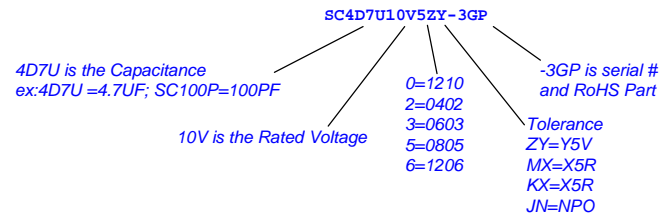
## Resistor



## Processor Strapping

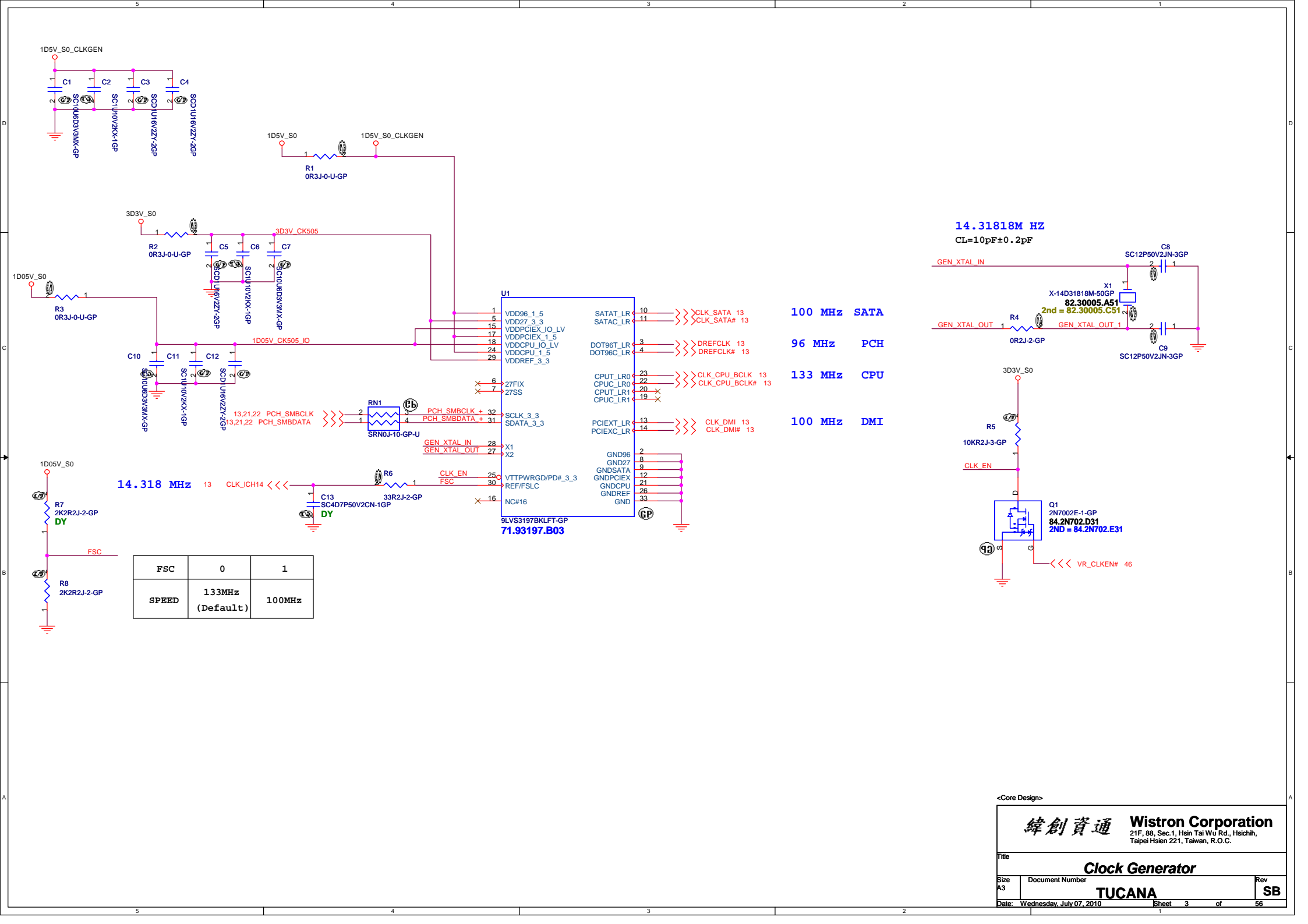
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	<b>Embedded DisplayPort Presence</b>	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	<b>PCI-Express Static Lane Reversal</b>	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	<b>PCI-Express Configuration Select</b>	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	<b>Reserved - Temporarily used for early Clarksfield samples.</b>	<b>Clarksfield (only for early samples pre-ES1) -</b> Connect to GND with 3.01K Ohm/5% resistor <b>Note:</b> Only temporary for early CFD samples (xPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

## Capacitor

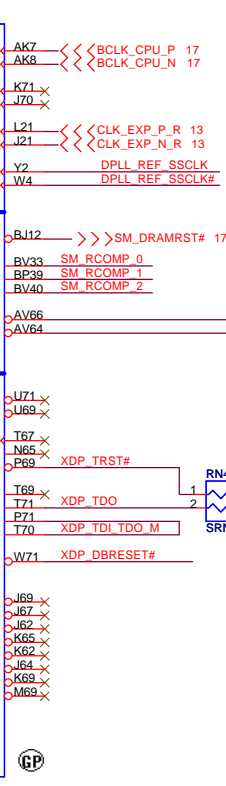
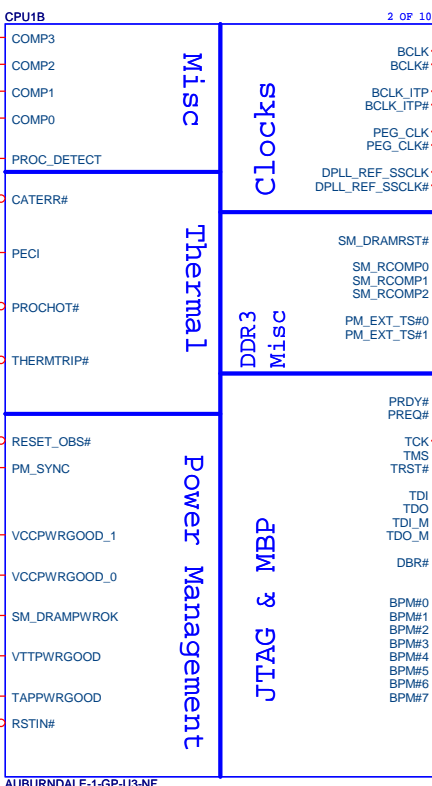
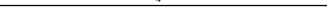
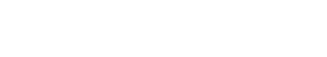
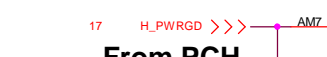
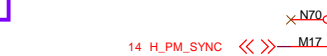
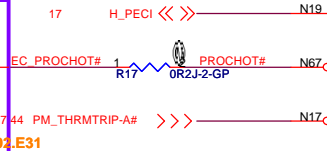
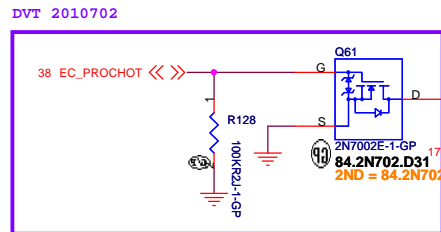
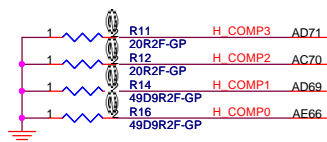
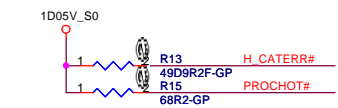


DVT 1ST

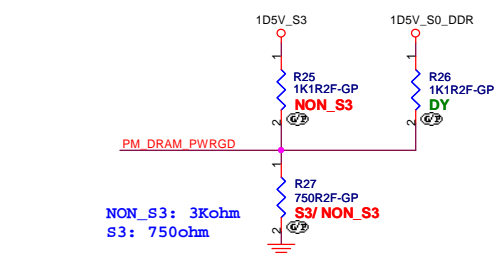
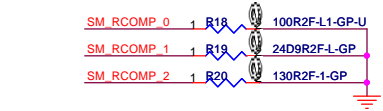
緯創資通		Wistron Corporation	
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Title			
Reference			
Size A3	Document Number	TUCANA	Rev SB
Date: Wednesday, July 07, 2010			
Sheet 2		of 56	







If supports integrated graphics but without Embedded DisplayPort(eDP), these pins can also be connected to GND directly.



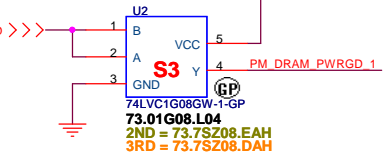
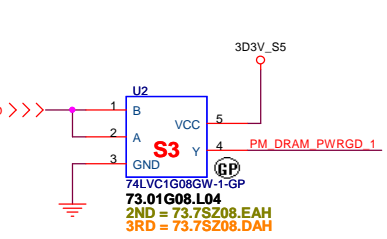
NON\_S3: 3Kohm  
S3: 750ohm

NON\_S3: 3Kohm  
S3: 750ohm

NON\_S3: 3Kohm  
S3: 750ohm

NON\_S3: 3Kohm  
S3: 750ohm

NON\_S3: 3Kohm  
S3: 750ohm



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Title		CPU SFF 2 of 8(CLK/Thermal)	
Size	Document Number	Rev	
A3		SB	
Date: Wednesday, July 07, 2010		Sheet 5 of 56	

21 M\_A\_DQ[63..0] <<>>

M A DQ0	AT8	SA_DQ0
M A DQ1	AT6	SA_DQ1
M A DQ2	BB5	SA_DQ2
M A DQ3	BB5	SA_DQ3
M A DQ4	AV7	SA_DQ4
M A DQ5	AV6	SA_DQ5
M A DQ6	BE6	SA_DQ6
M A DQ7	BE8	SA_DQ7
M A DQ8	BE11	SA_DQ8
M A DQ9	BE11	SA_DQ9
M A DQ10	BK5	SA_DQ10
M A DQ11	BH13	SA_DQ11
M A DQ12	BF9	SA_DQ12
M A DQ13	BF6	SA_DQ13
M A DQ14	BK7	SA_DQ14
M A DQ15	BN8	SA_DQ15
M A DQ16	BN11	SA_DQ16
M A DQ17	BN9	SA_DQ17
M A DQ18	BG17	SA_DQ18
M A DQ19	BK15	SA_DQ19
M A DQ20	BK9	SA_DQ20
M A DQ21	BG15	SA_DQ21
M A DQ22	BH17	SA_DQ22
M A DQ23	BK17	SA_DQ23
M A DQ24	BN20	SA_DQ24
M A DQ25	BN17	SA_DQ25
M A DQ26	BK25	SA_DQ26
M A DQ27	BH25	SA_DQ27
M A DQ28	BJ20	SA_DQ28
M A DQ29	BH21	SA_DQ29
M A DQ30	BG24	SA_DQ30
M A DQ31	BG25	SA_DQ31
M A DQ32	BJ40	SA_DQ32
M A DQ33	BM43	SA_DQ33
M A DQ34	BF47	SA_DQ34
M A DQ35	BF48	SA_DQ35
M A DQ36	BN40	SA_DQ36
M A DQ37	BH43	SA_DQ37
M A DQ38	BN44	SA_DQ38
M A DQ39	BN47	SA_DQ39
M A DQ40	BN48	SA_DQ40
M A DQ41	BN51	SA_DQ41
M A DQ42	BH53	SA_DQ42
M A DQ43	BJ55	SA_DQ43
M A DQ44	BH48	SA_DQ44
M A DQ45	BJ48	SA_DQ45
M A DQ46	BM53	SA_DQ46
M A DQ47	BN55	SA_DQ47
M A DQ48	BF55	SA_DQ48
M A DQ49	BN57	SA_DQ49
M A DQ50	BN65	SA_DQ50
M A DQ51	BJ61	SA_DQ51
M A DQ52	BF57	SA_DQ52
M A DQ53	BJ57	SA_DQ53
M A DQ54	BK64	SA_DQ54
M A DQ55	BK61	SA_DQ55
M A DQ56	BJ63	SA_DQ56
M A DQ57	BF64	SA_DQ57
M A DQ58	BB64	SA_DQ58
M A DQ59	BB66	SA_DQ59
M A DQ60	BJ66	SA_DQ60
M A DQ61	BF65	SA_DQ61
M A DQ62	AY64	SA_DQ62
M A DQ63	BC70	SA_DQ63

21 M\_A\_BS\_0 <<>> BT38  
21 M\_A\_BS\_1 <<>> BH38  
21 M\_A\_BS\_2 <<>> BF21

21 M\_A\_CAS# <<>> BK43C  
21 M\_A\_RAS# <<>> BL38C  
21 M\_A\_WE# <<>> BF38C

DDR SYSTEM MEMORY A

SA_CK0	BM34	M_CLK_DDR0 21
SA_CK#0	BP35	M_CLK_DDR#0 21
SA_CKE0	BF20	M_CKE0 21
SA_CK1	BK36	M_CLK_DDR1 21
SA_CK#1	BH36	M_CLK_DDR#1 21
SA_CKE1	BK24	M_CKE1 21
SA_CS#0	BH40	M_CS#0 21
SA_CS#1	BJ47	M_CS#1 21
SA_ODT0	BF43	M_ODT0 21
SA_ODT1	BL47	M_ODT1 21
SA_DM0	BB10	M_A_DM0
SA_DM1	BJ10	M_A_DM1
SA_DM2	BM15	M_A_DM2
SA_DM3	BN24	M_A_DM3
SA_DM4	BG44	M_A_DM4
SA_DM5	BG53	M_A_DM5
SA_DM6	BN62	M_A_DM6
SA_DM7	BH59	M_A_DM7
SA_DQS#0	AY5	M_A_DQS#0
SA_DQS#1	BJ7	M_A_DQS#1
SA_DQS#2	BN13	M_A_DQS#2
SA_DQS#3	BL21	M_A_DQS#3
SA_DQS#4	BH44	M_A_DQS#4
SA_DQS#5	BK51	M_A_DQS#5
SA_DQS#6	BP58	M_A_DQS#6
SA_DQS#7	BE62	M_A_DQS#7
SA_DQS0	AY7	M_A_DQS0
SA_DQS1	BJ5	M_A_DQS1
SA_DQS2	BL13	M_A_DQS2
SA_DQS3	BN21	M_A_DQS3
SA_DQS4	BK44	M_A_DQS4
SA_DQS5	BH51	M_A_DQS5
SA_DQS6	BM60	M_A_DQS6
SA_DQS7	BE64	M_A_DQS7
SA_MA0	BT36	M_A_A0
SA_MA1	BP33	M_A_A1
SA_MA2	BV36	M_A_A2
SA_MA3	BG34	M_A_A3
SA_MA4	BG32	M_A_A4
SA_MA5	BN32	M_A_A5
SA_MA6	BK32	M_A_A6
SA_MA7	BJ30	M_A_A7
SA_MA8	BN30	M_A_A8
SA_MA9	BF28	M_A_A9
SA_MA10	BH34	M_A_A10
SA_MA11	BH30	M_A_A11
SA_MA12	BJ28	M_A_A12
SA_MA13	BF40	M_A_A13
SA_MA14	BN28	M_A_A14
SA_MA15	BN25	M_A_A15



AUBURDALE-1-GP-U3-NF

22 M\_B\_DQ[63..0] <<>>

M_B_DQ0	BA2
M_B_DQ1	AW2
M_B_DQ2	BD1
M_B_DQ3	BE4
M_B_DQ4	AY1
M_B_DQ5	BQ2
M_B_DQ6	BF2
M_B_DQ7	BH2
M_B_DQ8	BG4
M_B_DQ9	BG1
M_B_DQ10	BR6
M_B_DQ11	BR8
M_B_DQ12	BJ4
M_B_DQ13	BK2
M_B_DQ14	BJ9
M_B_DQ15	BV10
M_B_DQ16	BR10
M_B_DQ17	BT12
M_B_DQ18	BT15
M_B_DQ19	BV15
M_B_DQ20	BV12
M_B_DQ21	BP12
M_B_DQ22	BV17
M_B_DQ23	BU16
M_B_DQ24	BP15
M_B_DQ25	BU19
M_B_DQ26	BV22
M_B_DQ27	BT22
M_B_DQ28	BP19
M_B_DQ29	BV19
M_B_DQ30	BV20
M_B_DQ31	BT20
M_B_DQ32	BT48
M_B_DQ33	BV48
M_B_DQ34	BV50
M_B_DQ35	BP49
M_B_DQ36	BT47
M_B_DQ37	BV52
M_B_DQ38	BV54
M_B_DQ39	BT54
M_B_DQ40	BP53
M_B_DQ41	BU53
M_B_DQ42	BT59
M_B_DQ43	BT57
M_B_DQ44	BP56
M_B_DQ45	BT55
M_B_DQ46	BU60
M_B_DQ47	BV59
M_B_DQ48	BV61
M_B_DQ49	BP60
M_B_DQ50	BR66
M_B_DQ51	BR64
M_B_DQ52	BR62
M_B_DQ53	BT61
M_B_DQ54	BN68
M_B_DQ55	BL69
M_B_DQ56	BJ71
M_B_DQ57	BF70
M_B_DQ58	BG71
M_B_DQ59	BC67
M_B_DQ60	BK70
M_B_DQ61	BK67
M_B_DQ62	BD71
M_B_DQ63	BD69

22 M\_B\_BS\_0 <<>> BV43  
22 M\_B\_BS\_1 <<>> BV41  
22 M\_B\_BS\_2 <<>> BV24

22 M\_B\_CAS# <<>> BU46C  
22 M\_B\_RAS# <<>> BT40C  
22 M\_B\_WE# <<>> BT41C

DDR SYSTEM MEMORY - B

SB_CK0	BU33	M_CLK_DDR2 22
SB_CK#0	BV34	M_CLK_DDR#2 22
SB_CKE0	BT26	M_CKE2 22
SB_CK1	BV38	M_CLK_DDR3 22
SB_CK#1	BU39	M_CLK_DDR#3 22
SB_CKE1	BT24	M_CKE3 22
SB_CS#0	BP46	M_CS#2 22
SB_CS#1	BT43	M_CS#3 22
SB_ODT0	BV45	M_ODT2 22
SB_ODT1	BU49	M_ODT3 22
SB_DM0	BB4	M_B_DM0
SB_DM1	BL4	M_B_DM1
SB_DM2	BT13	M_B_DM2
SB_DM3	BP22	M_B_DM3
SB_DM4	BV47	M_B_DM4
SB_DM5	BV57	M_B_DM5
SB_DM6	BU65	M_B_DM6
SB_DM7	BF67	M_B_DM7
SB_DQS#0	BE2	M_B_DQS#0
SB_DQS#1	BM3	M_B_DQS#1
SB_DQS#2	BU12	M_B_DQS#2
SB_DQS#3	BT19	M_B_DQS#3
SB_DQS#4	BT52	M_B_DQS#4
SB_DQS#5	BV55	M_B_DQS#5
SB_DQS#6	BU63	M_B_DQS#6
SB_DQS#7	BG69	M_B_DQS#7
SB_DQS0	BD4	M_B_DQS0
SB_DQS1	BN4	M_B_DQS1
SB_DQS2	BV13	M_B_DQS2
SB_DQS3	BT17	M_B_DQS3
SB_DQS4	BT50	M_B_DQS4
SB_DQS5	BU56	M_B_DQS5
SB_DQS6	BV62	M_B_DQS6
SB_DQS7	BJ69	M_B_DQS7
SB_MA0	BT34	M_B_A0
SB_MA1	BP30	M_B_A1
SB_MA2	BV29	M_B_A2
SB_MA3	BU30	M_B_A3
SB_MA4	BV31	M_B_A4
SB_MA5	BT33	M_B_A5
SB_MA6	BT31	M_B_A6
SB_MA7	BP26	M_B_A7
SB_MA8	BV27	M_B_A8
SB_MA9	BT27	M_B_A9
SB_MA10	BU42	M_B_A10
SB_MA11	BU26	M_B_A11
SB_MA12	BT29	M_B_A12
SB_MA13	BT45	M_B_A13
SB_MA14	BV26	M_B_A14
SB_MA15	BU23	M_B_A15



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Title

CPU SFF 3 of 8(DDR)

Size A3

Document Number

TUCANA

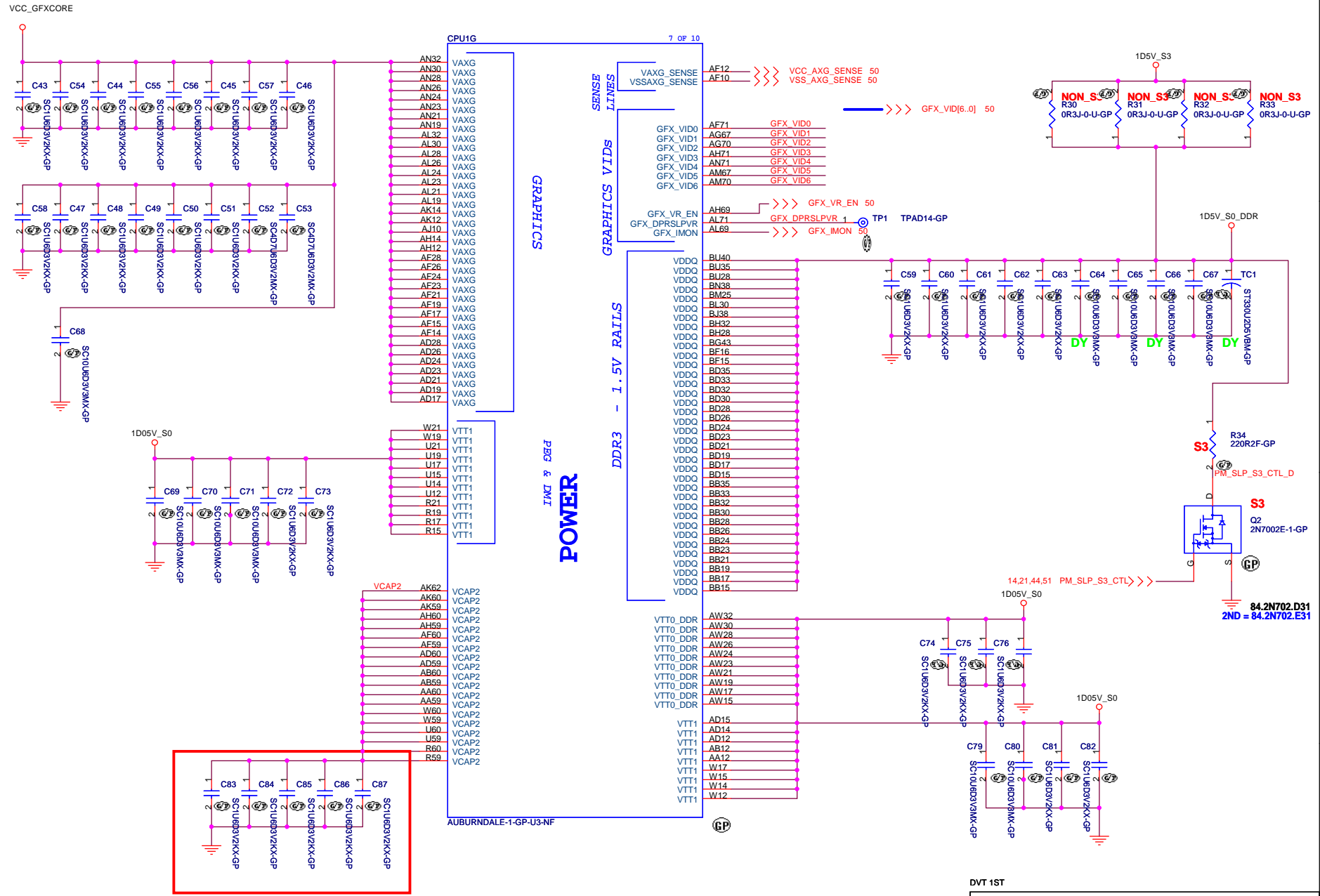
Rev

SB

Date: Wednesday, July 07, 2010

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Do not dummy these CAPS

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Title

CPU SFF 5 of 8(PWR/DDR/GFX/)

Size

A3

Document Number

TUCANA

Rev

SB

Date

Wednesday, July 07, 2010

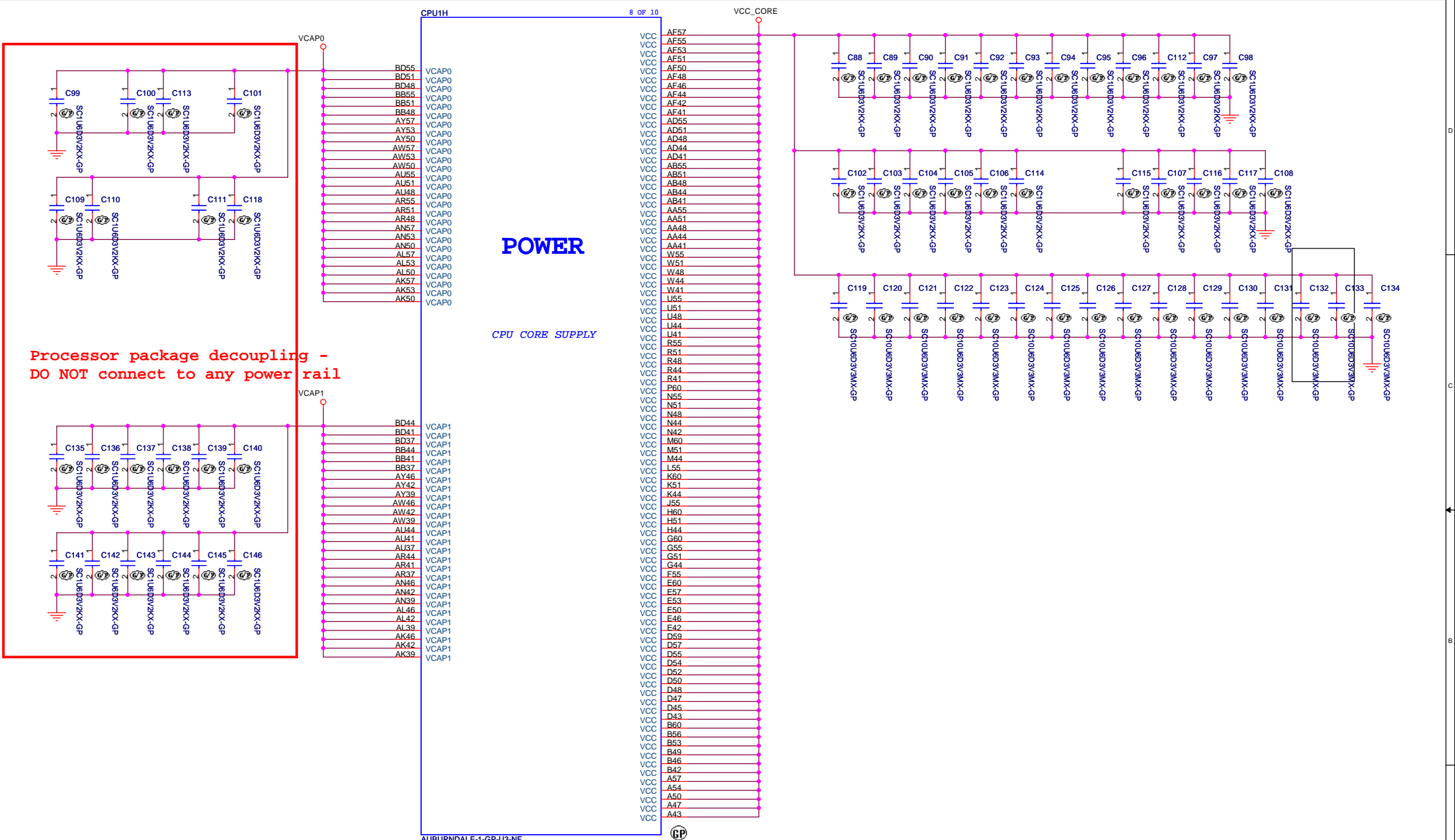
Sheet

8

of

56





CPU1E

5 OF 10

RSVD#W66  
RSVD#W64W66  
W64RSVD#AC69  
RSVD#AC71AC69  
AC71RSVD#AA71  
RSVD#AA69AA71  
AA69RSVD#R66  
RSVD#R64R66  
R64RSVD\_NCTF#BT5  
RSDV\_NCTF#BR5BT5  
BR5RSDV\_NCTF#BV6  
RSDV\_NCTF#BV8BV6  
BV8RSVD#AV69  
RSVD#AK71AV69  
AK71RSVD#AN69  
RSVD#AP66AN69  
AP66RSVD#AH66  
RSVD#AK66AH66  
AK66RSVD#AR71  
RSVD#AM66AR71  
AM66RSVD#AK69  
RSVD#AU71AK69  
AU71RSVD#AT70  
RSVD#AR69AT70  
AR69RSVD#AU69  
RSVD#AT67AU69  
AT67RSVD\_TP2  
RSVD\_TP1AP2  
AN7RSVD#AV4  
RSVD#AU2AV4  
AU2RSVD#BE69  
RSVD#BE71BE69  
BE71

RESERVED

RSVD\_TP0

RSVD#T4

RSVD#T2

RSVD#U1

RSVD#V2

RSVD#AV71

RSVD#AW70

RSVD#D8

RSVD#B7

RSVD#A10

RSVD#B9

RSVD\_NCTF#C5

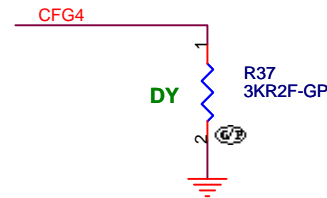
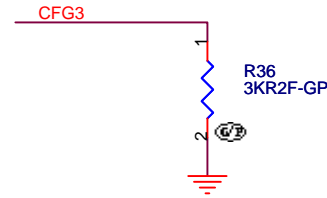
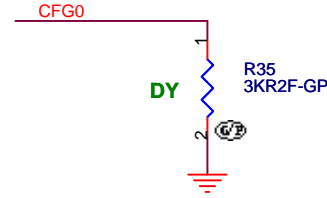
RSVD\_NCTF#A6

RSVD\_NCTF#E3

RSVD\_NCTF#F1

NCTF TEST PIN:  
A5,A68,A69,A71,C3,C71,E1,E71,BR1,BR71,  
BT1,BT71,BV1,BV3,BV5,BV68,BV69,BV71NCTF\_DC\_TEST#BV71  
NCTF\_DC\_TEST#BV69  
NCTF\_DC\_TEST#BV68NCTF\_DC\_TEST#BV5  
NCTF\_DC\_TEST#BV3  
NCTF\_DC\_TEST#BV1NCTF\_DC\_TEST#BT71  
DC\_TEST\_BT69  
DC\_TEST\_BT3NCTF\_DC\_TEST#BT1  
NCTF\_DC\_TEST#BR71  
NCTF\_DC\_TEST#BR1NCTF\_DC\_TEST#E71  
NCTF\_DC\_TEST#E1  
NCTF\_DC\_TEST#C71DC\_TEST\_C69  
NCTF\_DC\_TEST#C3  
NCTF\_DC\_TEST#A71NCTF\_DC\_TEST#A69  
NCTF\_DC\_TEST#A68  
NCTF\_DC\_TEST#A5BV71  
BV69  
BV68BV5  
BV3  
BV1BT71  
BT69  
BT3BT1  
BR71  
BR1E71  
E1  
C71C69  
C3  
A71A69  
A68  
A5

GP

TP2  
TPAD14-GPTP3  
TPAD14-GPTP4  
TPAD14-GPTP5  
TPAD14-GP

## PCI-Express Configuration Select

CFG0

1:Single PEG  
0:Bifurcation enabled

## CFG3 - PCI-Express Static Lane Reversal

CFG3

1 :Normal Operation  
0 :Lane Numbers Reversed  
15 -> 0, 14 -> 1, ...

## CFG4 - Display Port Presence

CFG4

1:Disabled; No Physical Display Port  
attached to Embedded Display Port  
0:Enabled; An external Display Port  
device is connected to the Embedded  
Display Port

DVT 1ST

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Title CPU SFF 7 of 8(REERVED)

Size A4 Document Number

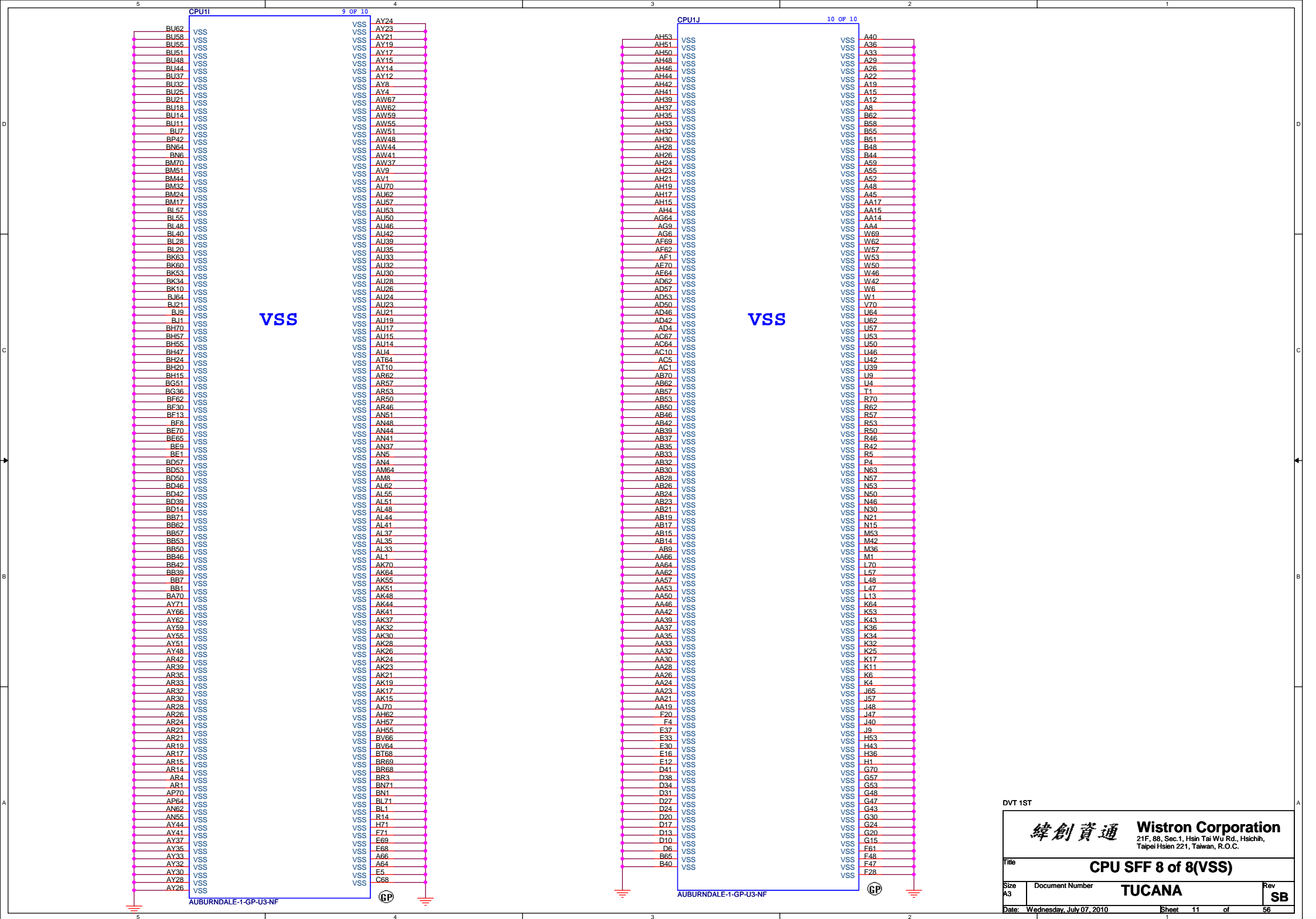
TUCANA

Rev

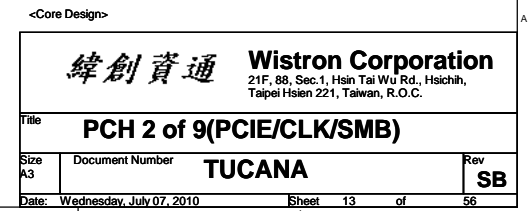
SB

Date: Wednesday, July 07, 2010

Sheet 10 of 56

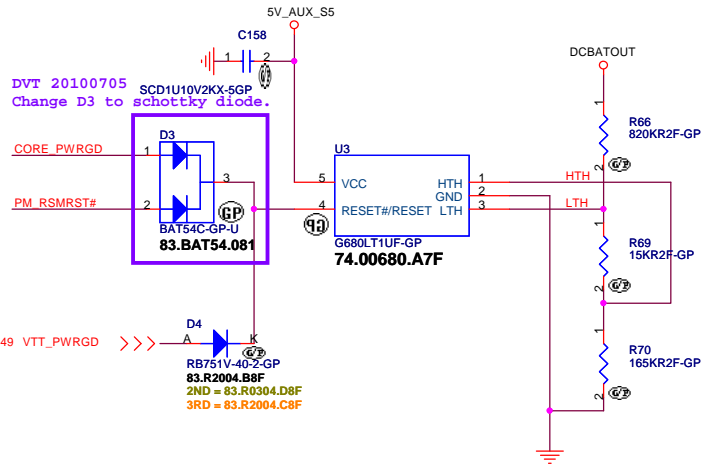






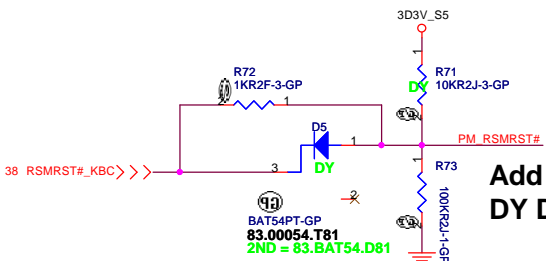


Delete PM\_PWRBTN# pull high

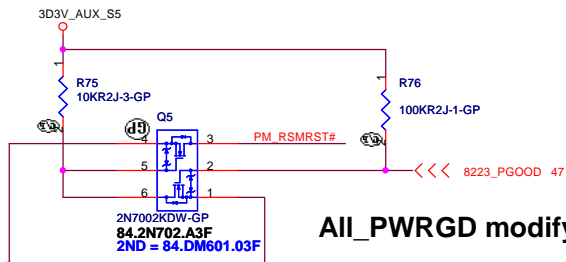


$$V_L = 1.245 \left( \frac{R1+R2+R3}{(R2+R3)} \right)$$

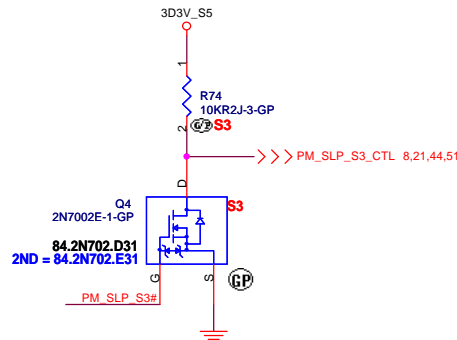
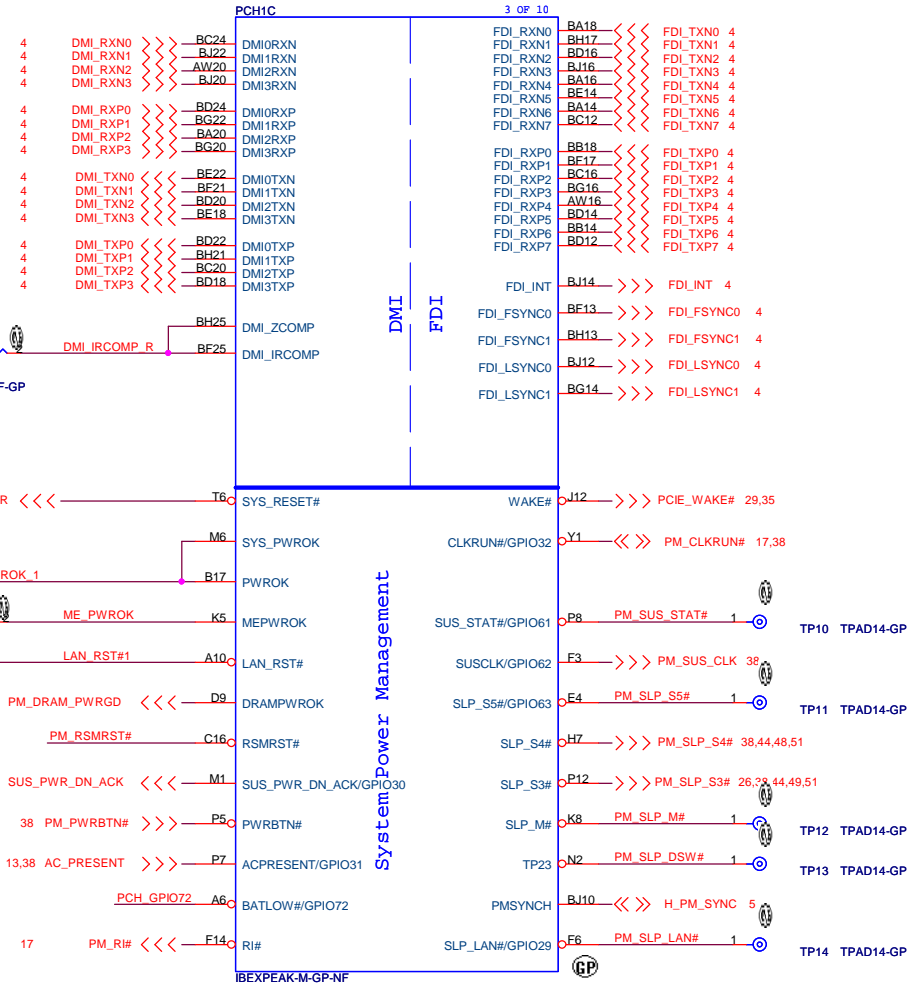
$$V_h = 1.245 \left( \frac{R1+R2+R3}{(R3)} \right)$$



Add RTC Data lose function  
DY D5



All\_PWRGD modify 51123\_PGOOD from 3V/5V power



DVT 1ST

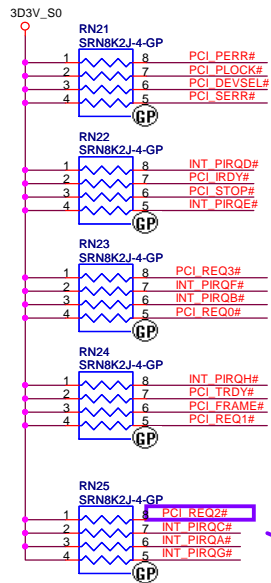
緯創資通 Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title			PCH 3 of 9(DMI/FDI)
Size	Document Number	TUCANA	
A3		Rev	
		SB	
Date:	Wednesday, July 07, 2010	Sheet	14 of 56

[illegible]

Title				<b>PCH 4 of 9(LVDS/CRT/DP)</b>			
Size Custom	Document Number					Rev	
	<b>TUCANA</b>					<b>SB</b>	
Date: Wednesday, July 07, 2010				Sheet	15	of	56



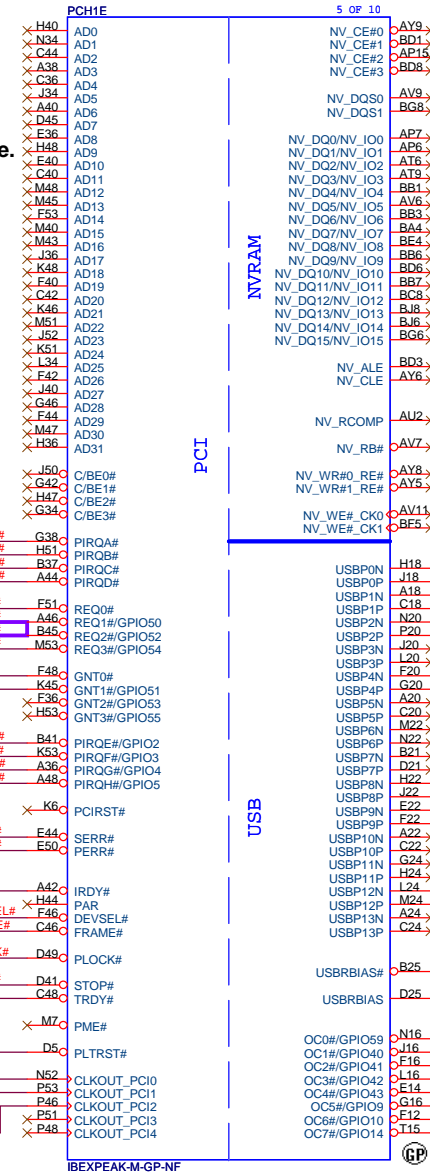
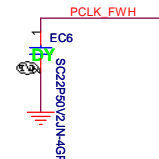
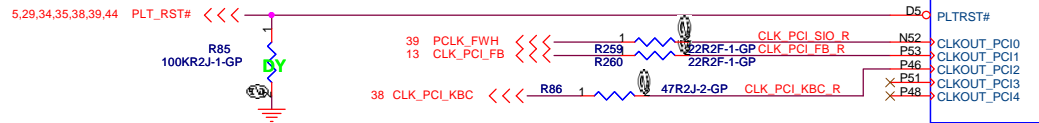


These pins are left as NC,  
because the function is disable.



BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI

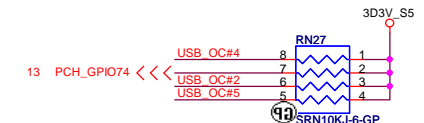
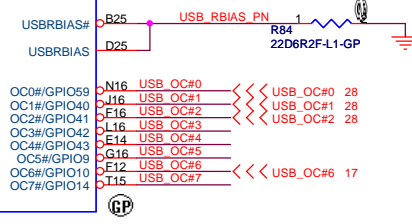
DVT 20100621  
Add PCI\_REQ2# Pull-High to 3D3V\_S0  
by hang-up issue



These pins are left as NC,  
because the function is disable.

## USB Table

Pair	Device
0	External #0
1	External #1
2	CardReader
3	NC
4	External #2
5	NC
6	NC
7	NC
8	WLAN/WiMAX
9	CAMERA(HS)
10	NC
11	NC
12	BLUETOOTH(FS)
13	NC



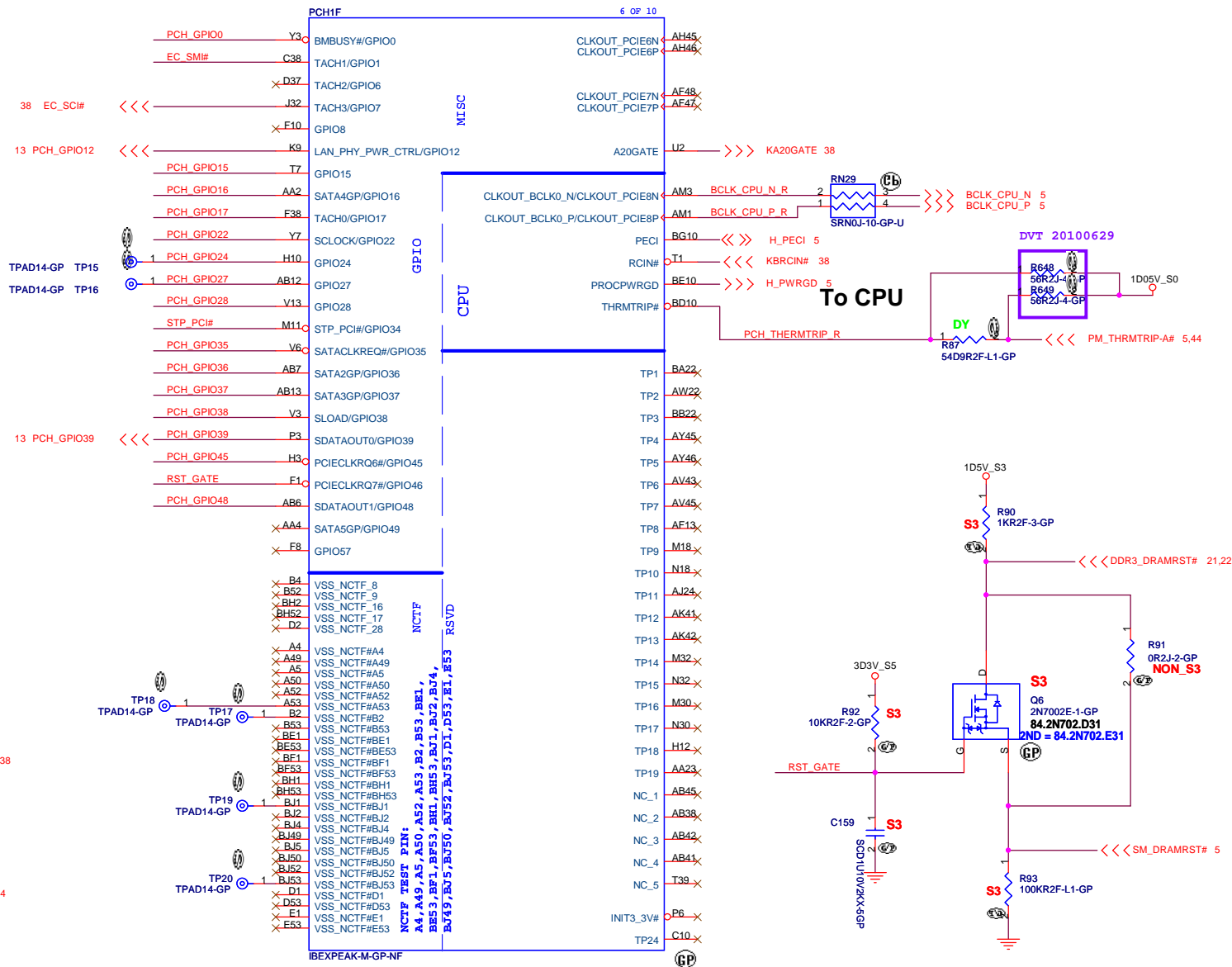
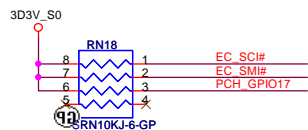
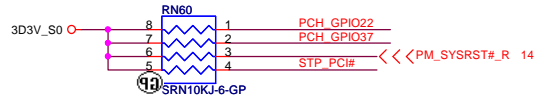
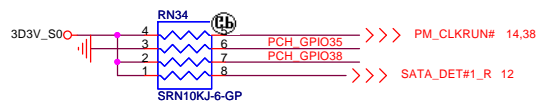
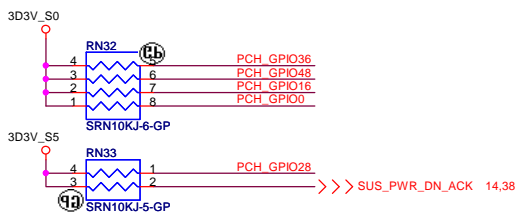
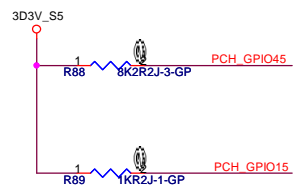
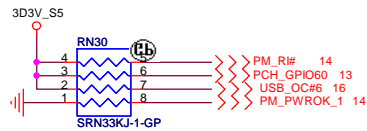
DVT 1ST

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Title PCH 5 of 9(PCI/USB)		
Size A3	Document Number TUCANA	Rev SB
Date: Wednesday, July 07, 2010	Sheet 16	of 56



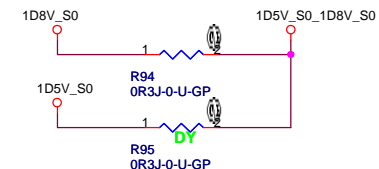
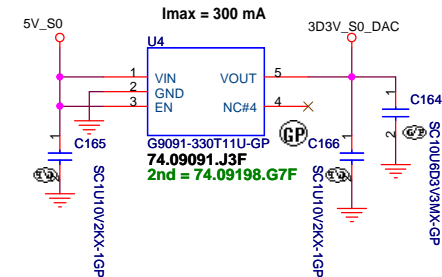
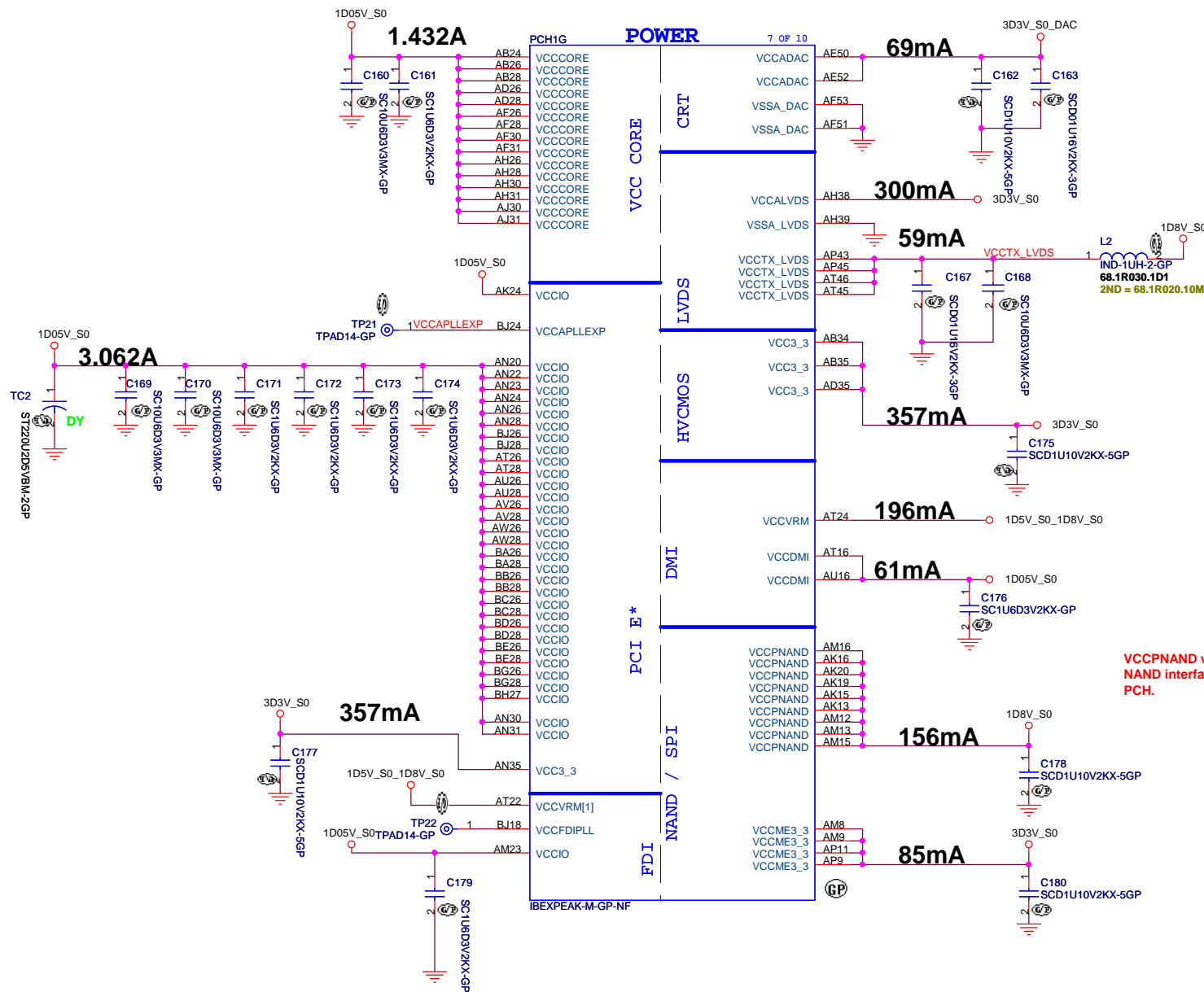
GPIO27 has a weak[20K] internal pull up.  
To enable on-die PLL Voltage regulator,  
should not place external pull down.



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Size A3	Document Number <b>TUCANA</b>	Rev <b>SB</b>
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Date: Wednesday, July 07, 2010 Sheet 17 of 56



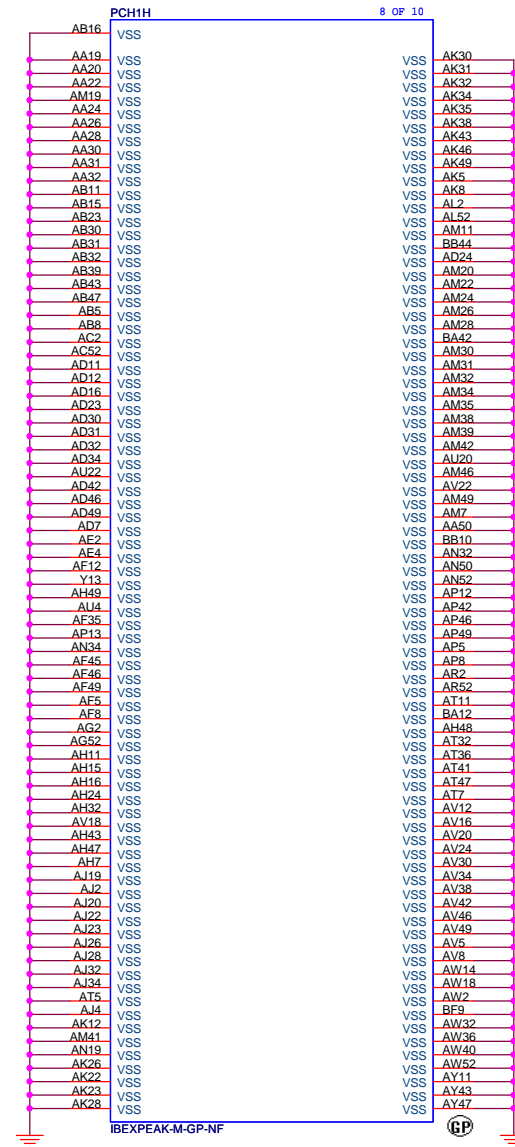
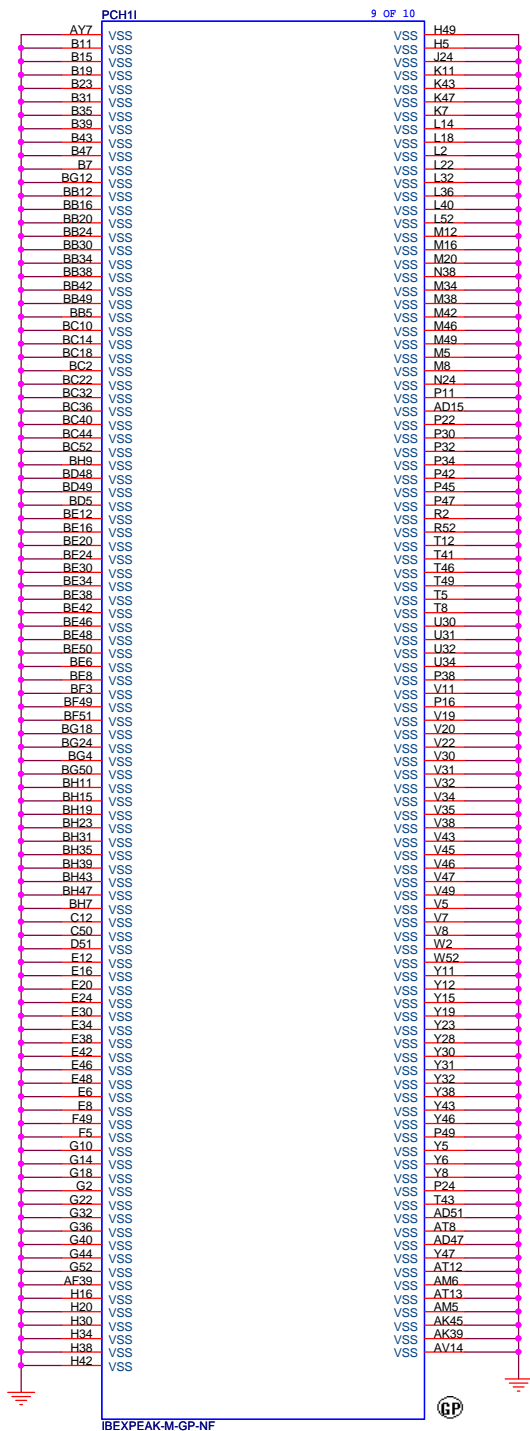
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

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Title <b>PCH 7 of 9(PWR/VCORE/LVDS)</b>		
Size Custom	Document Number <b>TUCANA</b>	Rev <b>SB</b>
Date: Wednesday, July 07, 2010	Sheet 18	of 56





DVT 1ST

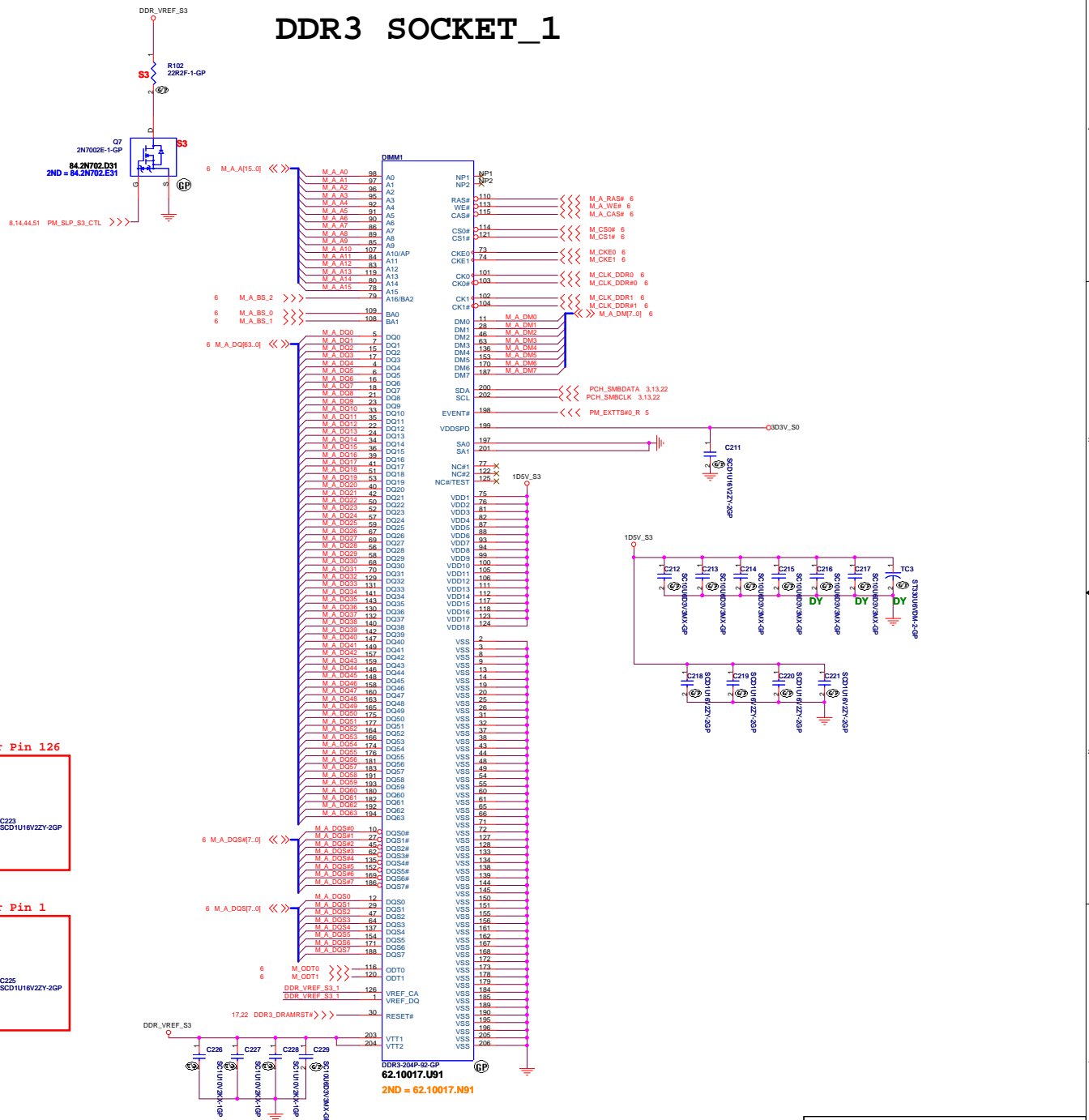
緯創資通 Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.


Title PCH 9 of 9(VSS)

Size A3 Document Number TUCANA Rev SB

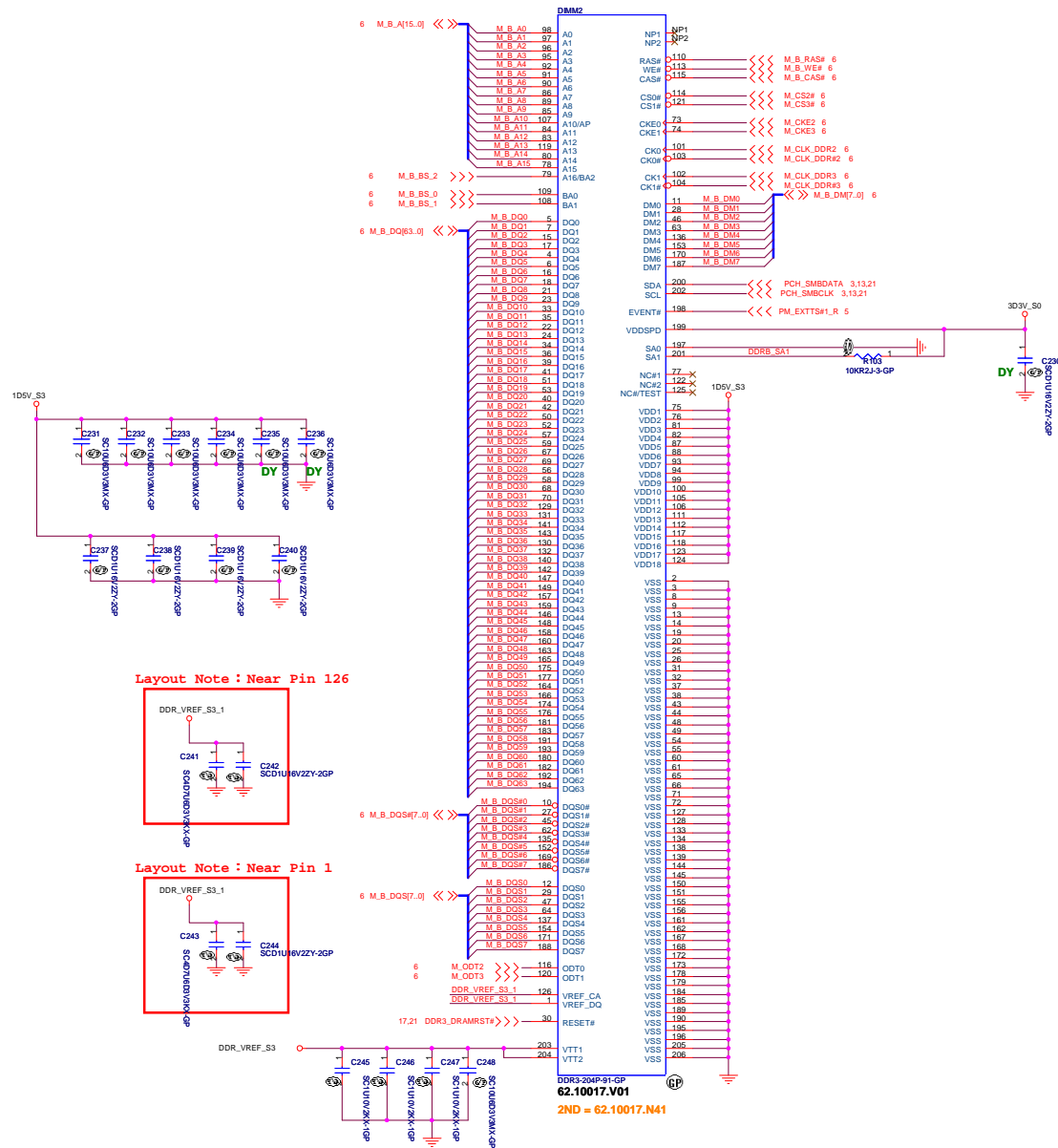
Date: Wednesday, July 07, 2010 Sheet 20 of 56

## DDR3 SOCKET\_1

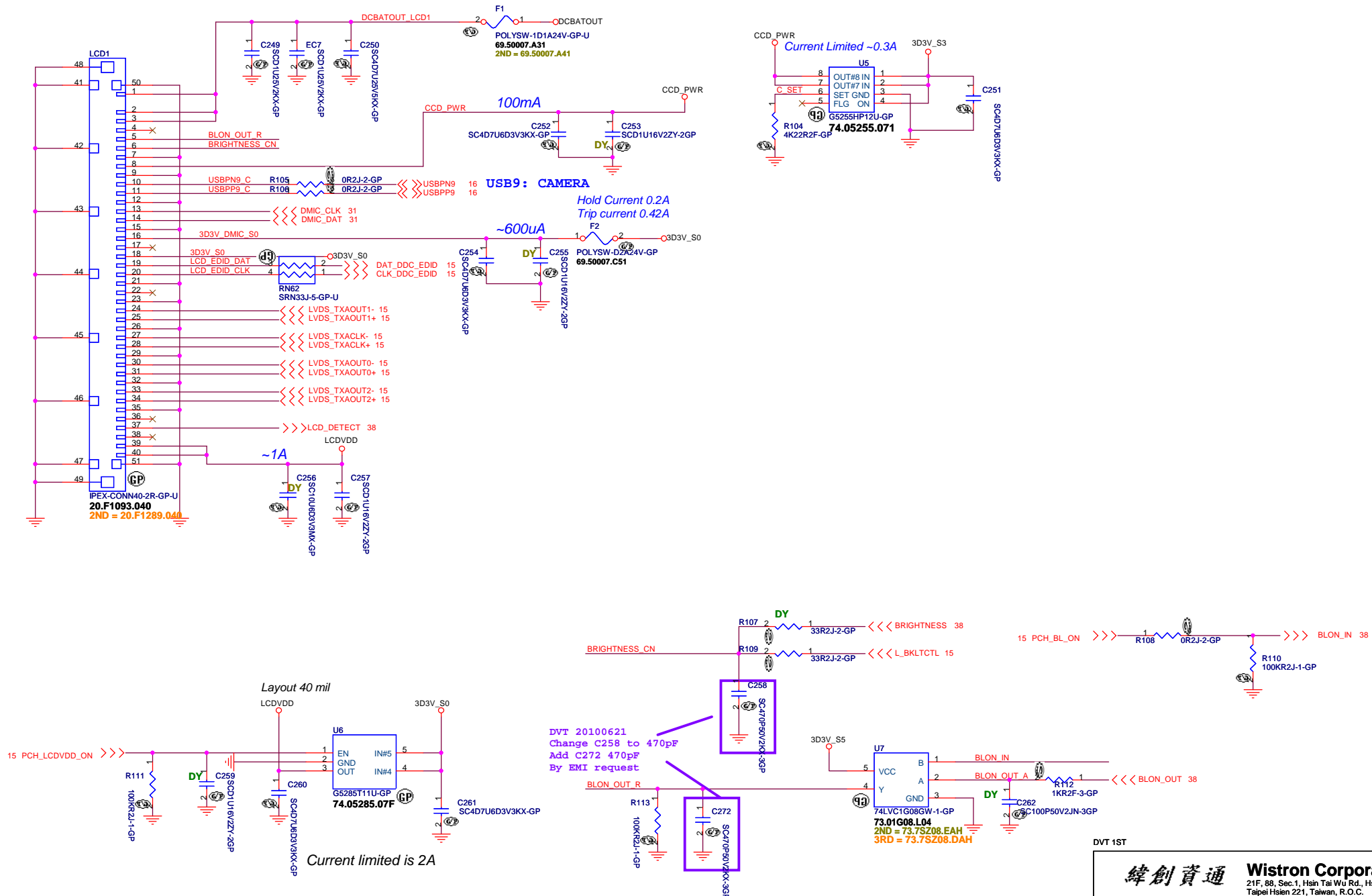


 <b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
		<b>DDR3 Socket1</b>	
Size	Document Number		Rev
<b>TUCANA</b>			SB
Date	Wednesday, July 07, 2010	Sheet	21 of 56

## DDR3 SOCKET\_2



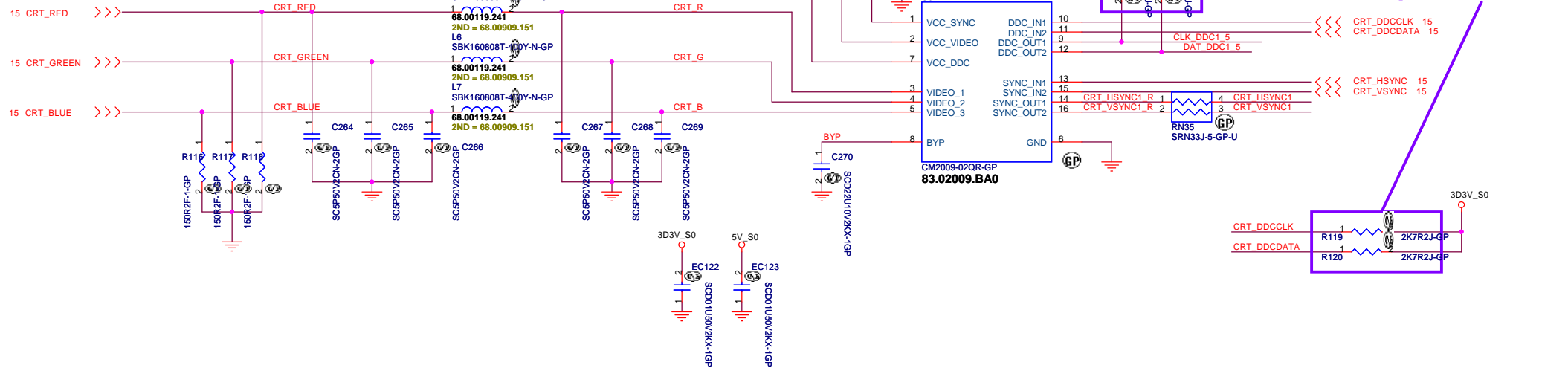
# LCD/CCD CONN



DVT 1ST

Layout Note:  
Place these resistors  
close to the CRT-out  
connector

Ferrite bead impedance: 40 ohm@100MHz

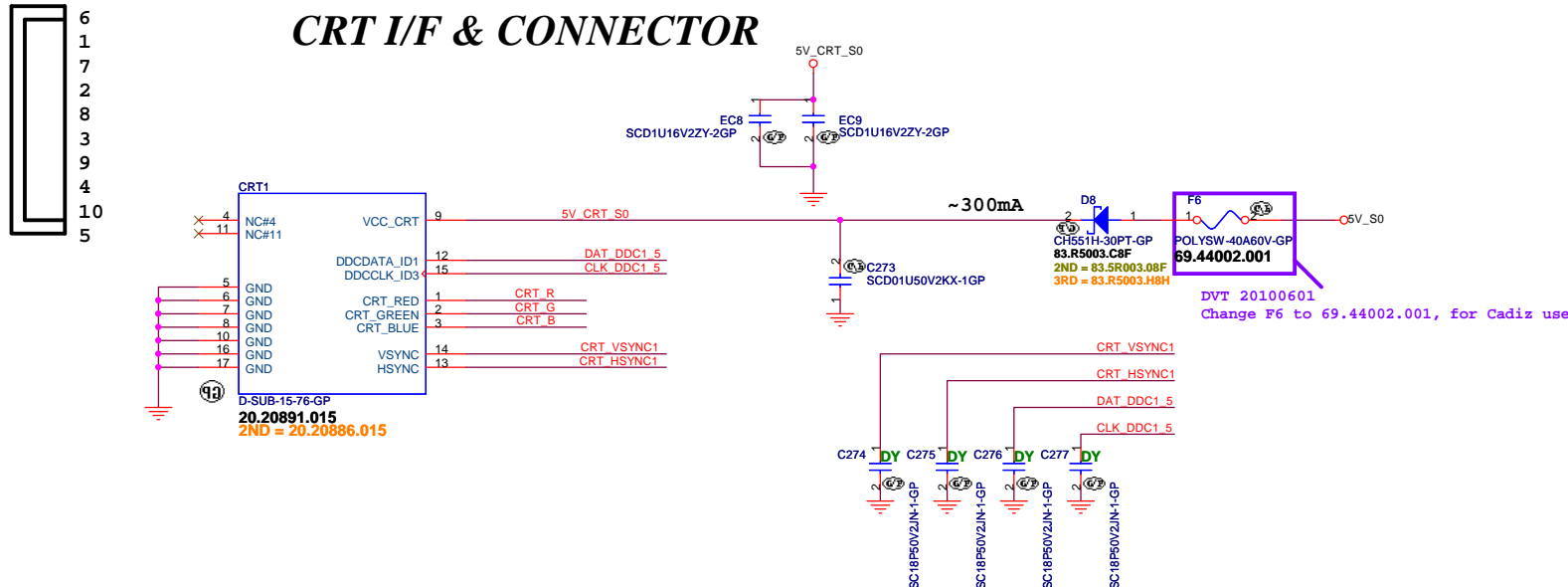


Layout Note:

\* Must be a ground return path between this ground and the ground on the VGA connector.

Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

## CRT I/F & CONNECTOR



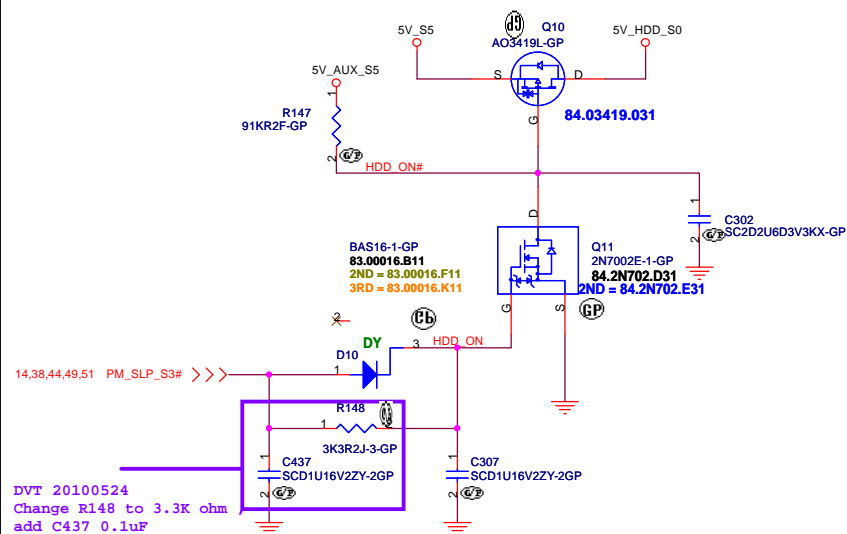
DVT 1ST

緯創資通 Wistron Corporation  
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Title			CRT CONN	
Size	Document Number		TUCANA	
Date: Wednesday, July 07, 2010	Sheet 24 of 56		Rev SB	

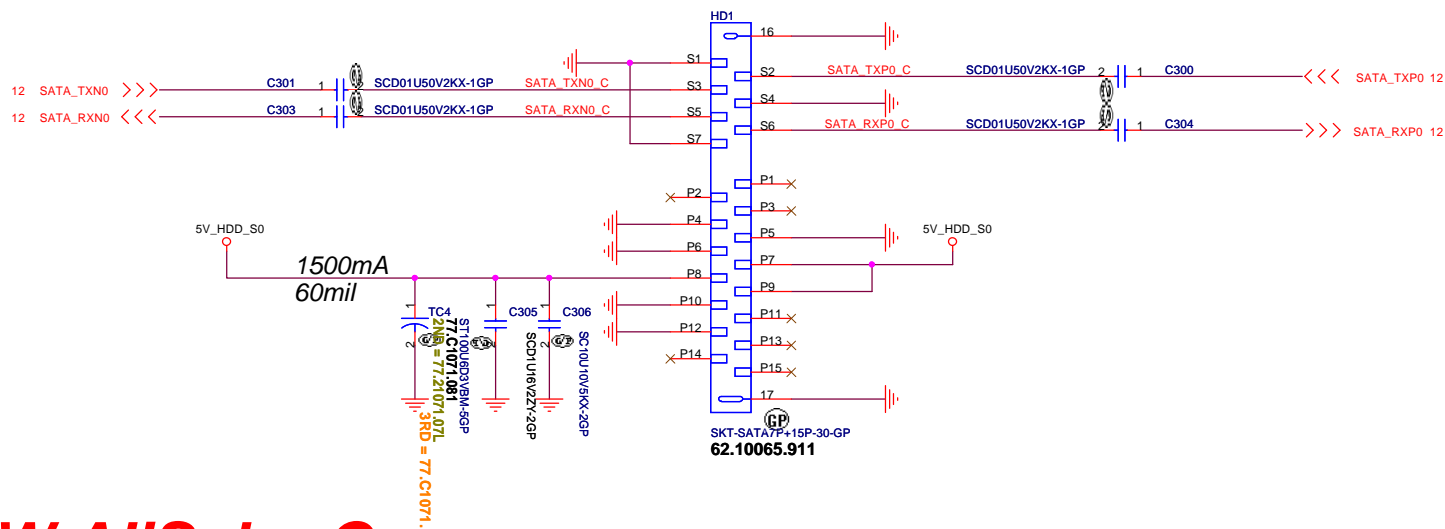






Delay HDD power off timing for 400ms after SATA controller shut down. Control the C307 and R148 to finally tune delay timing between 500ms and 400ms.

## SSD SATA Connector



<Core Design>

緯創資通

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Title

**HDD Connector**

Size

Document Number

**TUCANA**

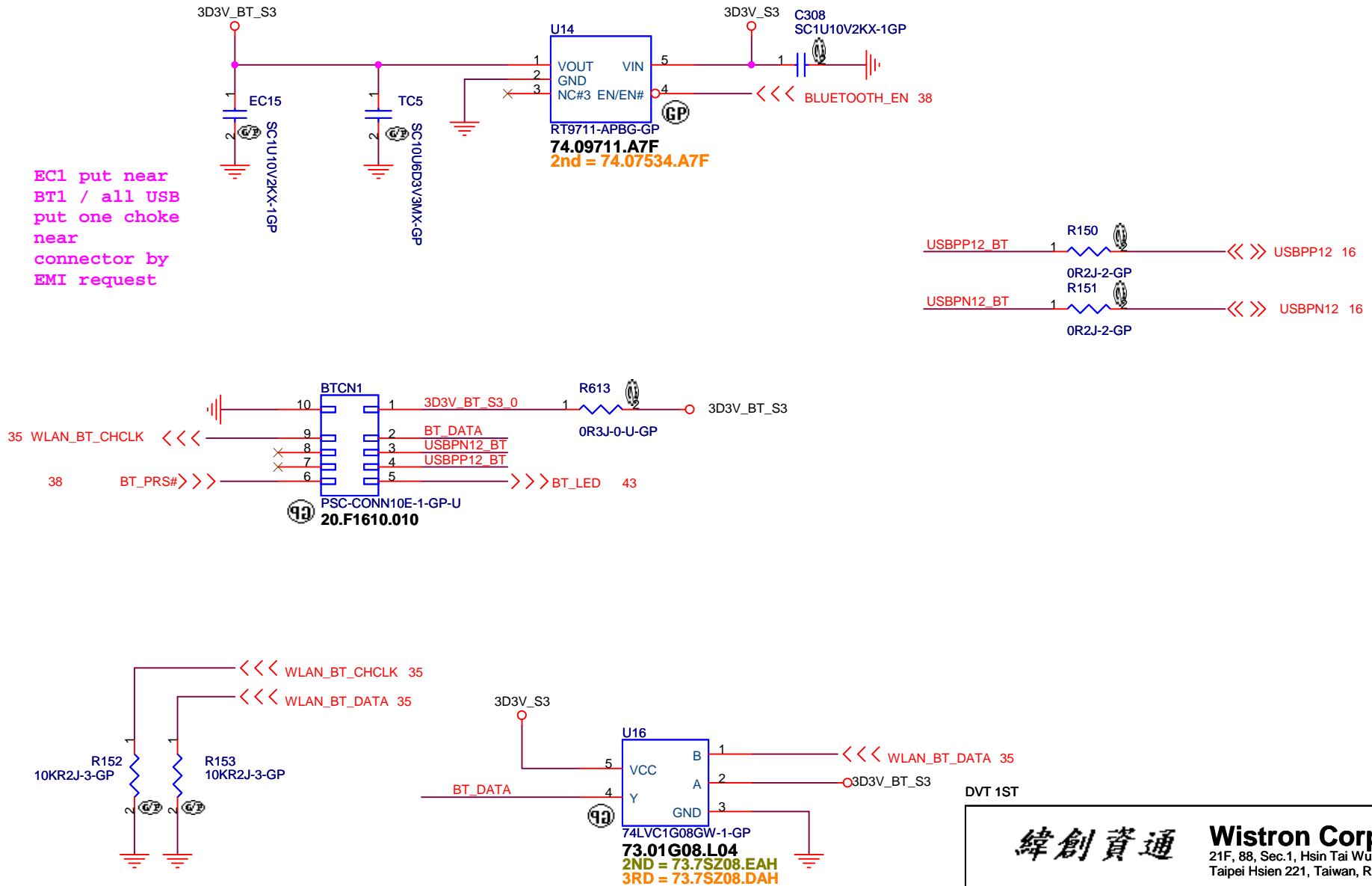
Rev

**SB**

Date: Wednesday, July 07, 2010

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# Bluetooth



DVT 1ST

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Bluetooth**

Size

Document Number

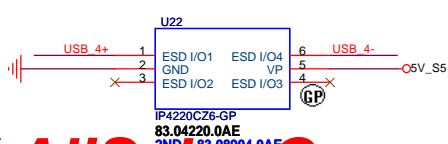
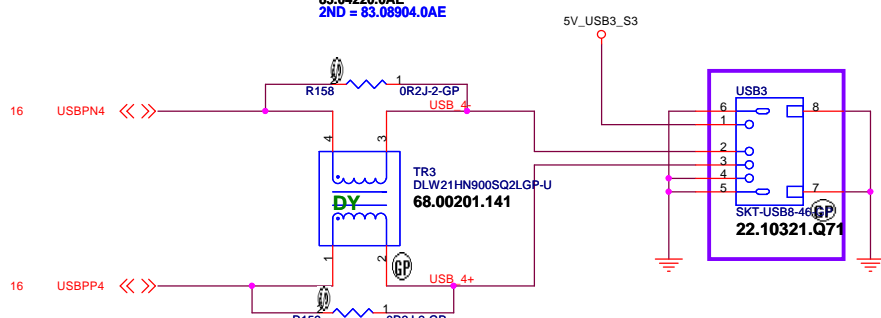
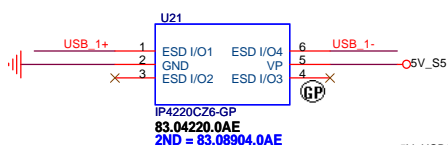
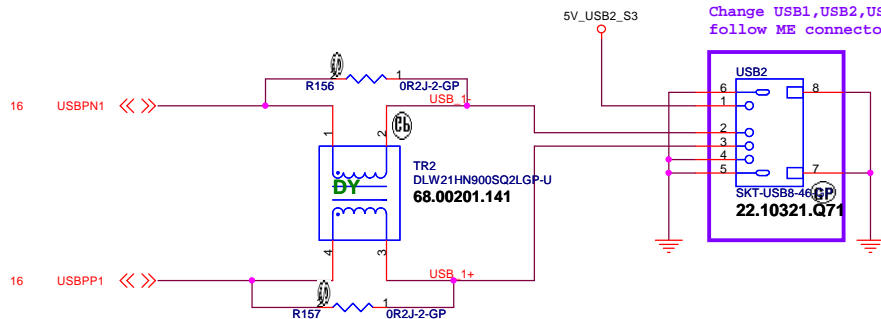
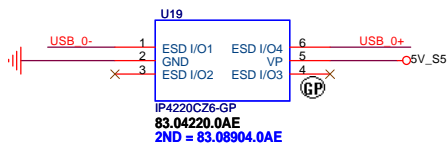
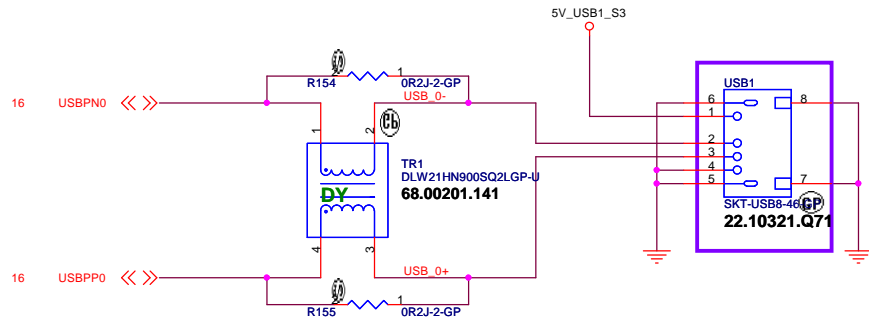
**TUCANA**

Rev

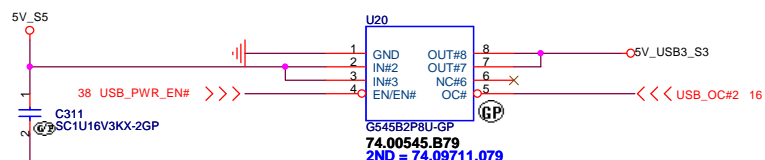
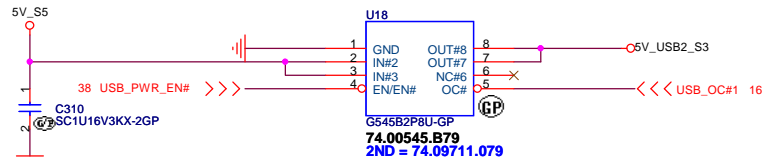
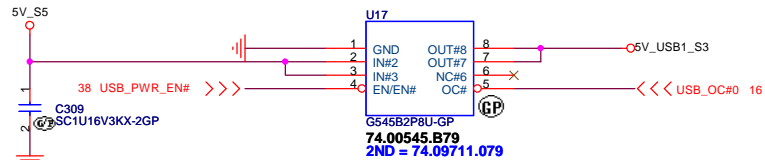
**SB**

Date: Wednesday, July 07, 2010

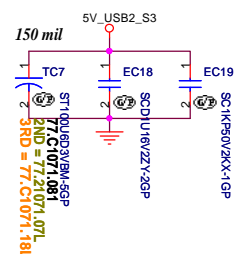
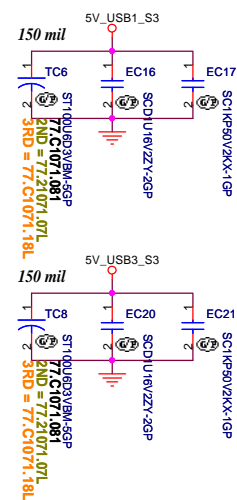
Sheet 27 of 56



DVT 20100604  
Change USB1,USB2,USB3 to 22.10321.Q71  
follow ME connector list.

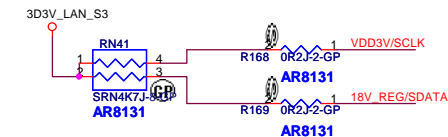
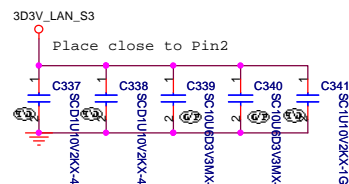
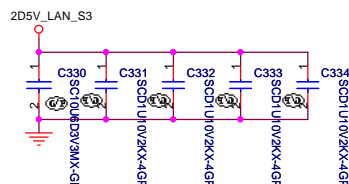
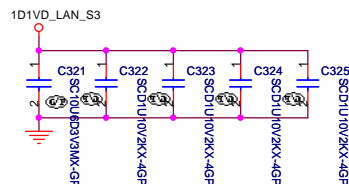
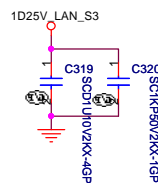
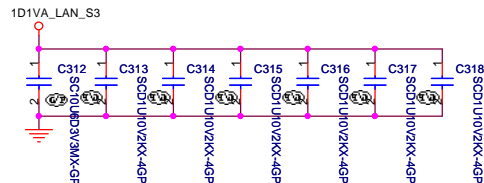


U17,U18,U20 Current Limit 1.5A

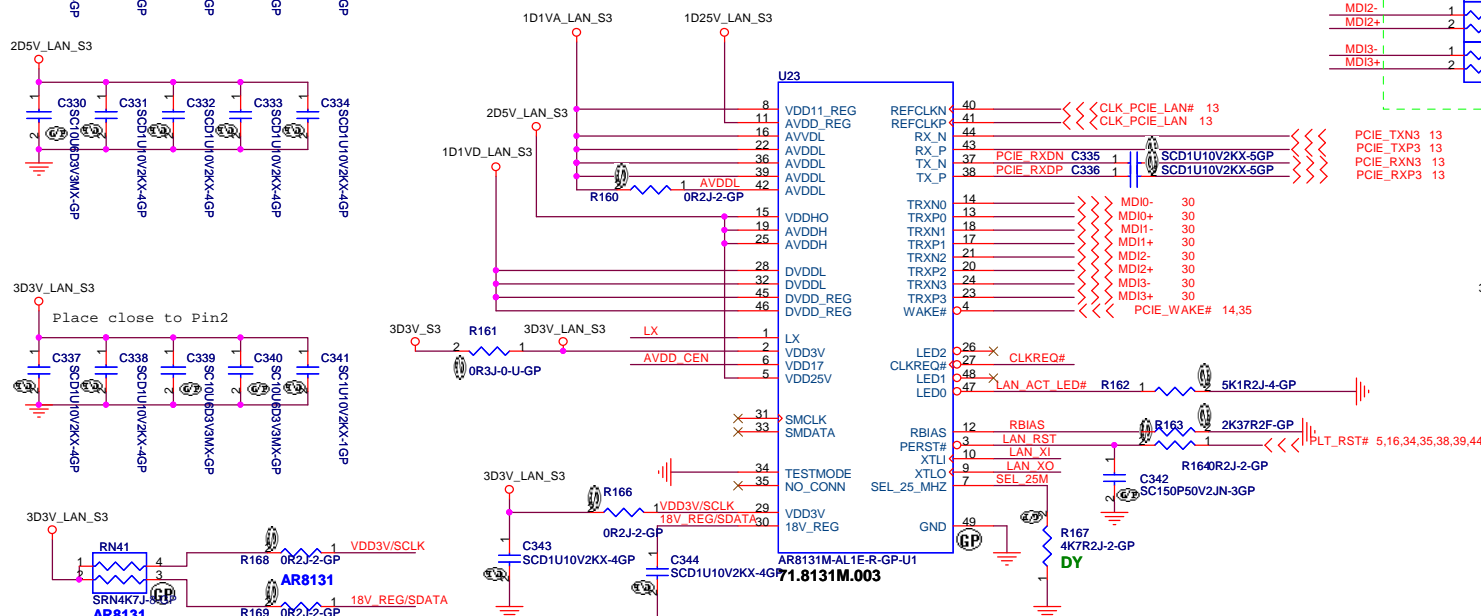
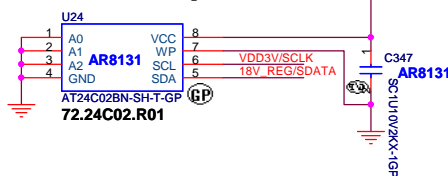


DVT 1ST

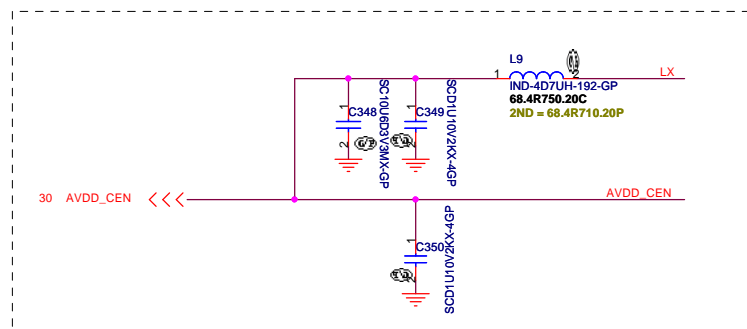
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: <b>USB CONN</b>		
Size	Document Number	Rev
<b>TUCANA</b>		<b>SB</b>
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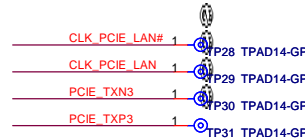
for AR8131 chip



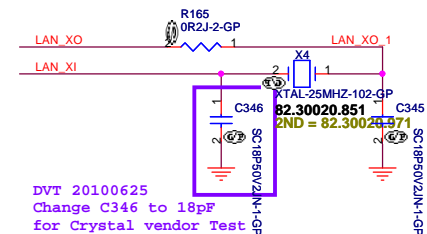
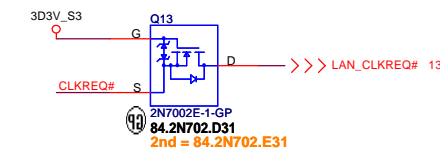
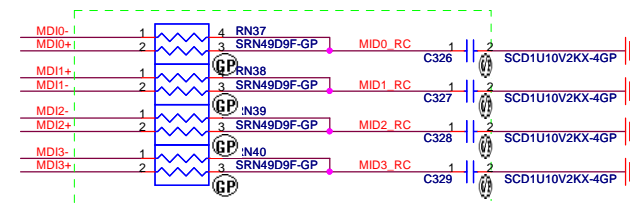
For AR8131: RN41,R168,R169,U24,C347 are need to stuff.  
For AR8131M: RN41,R168,R169,U24,C347 are DY



Close to U3



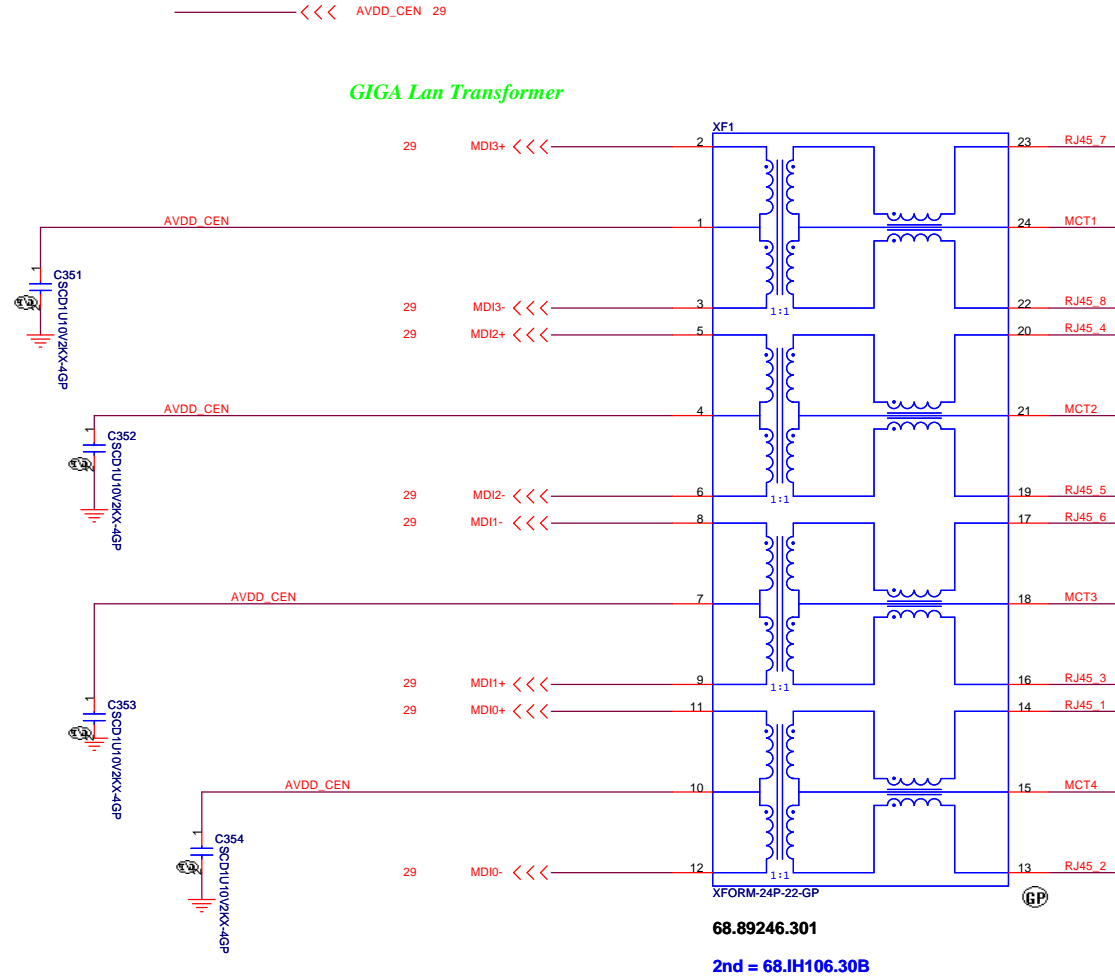
Close to LAN\_AR8131



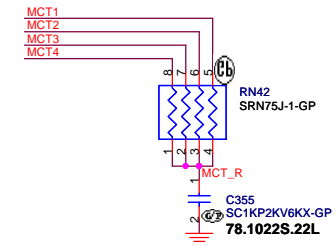
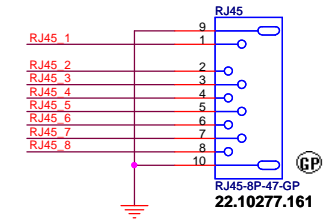
DVT 1ST

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

## LAN Transformer



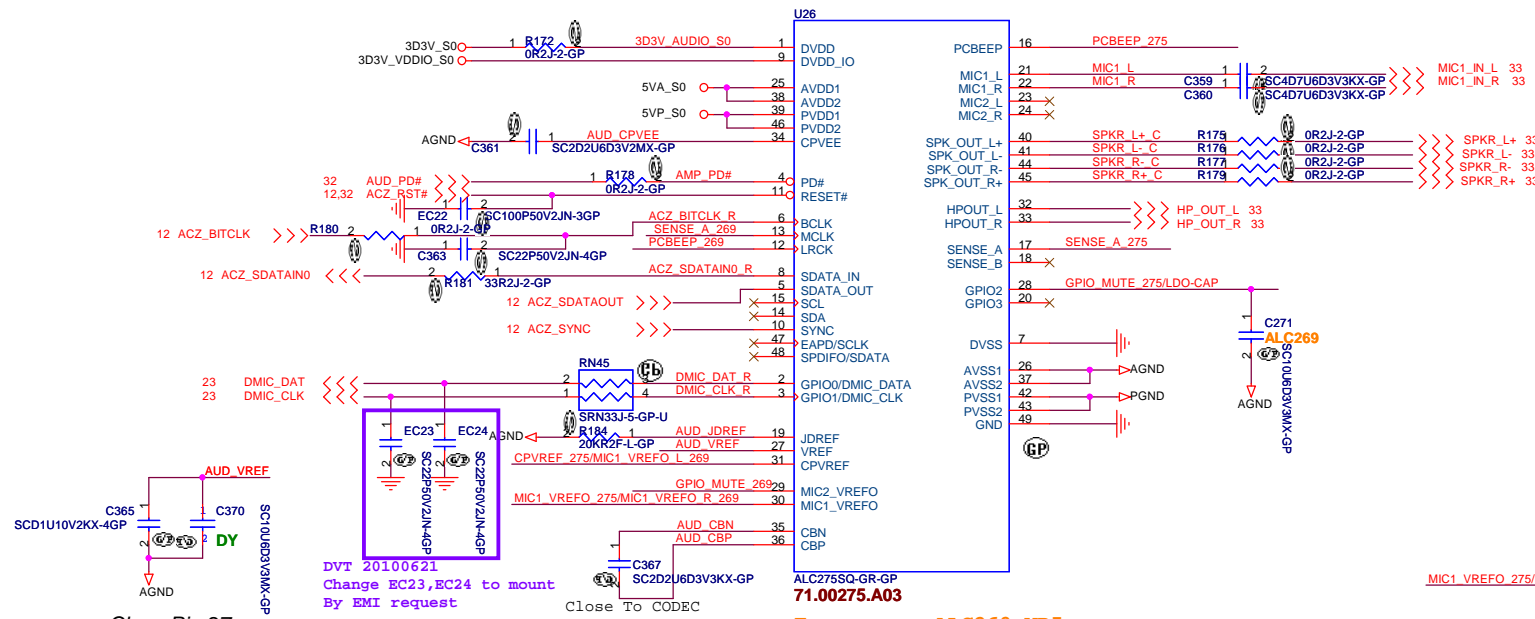
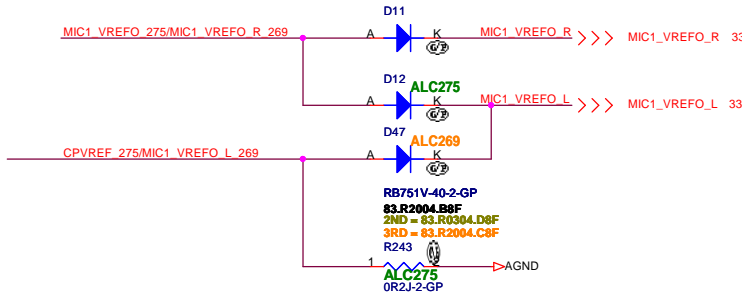
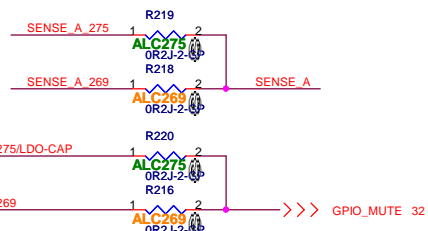
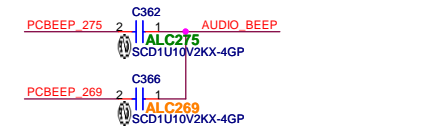
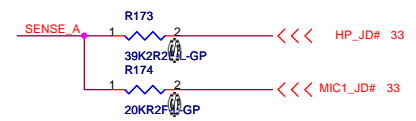
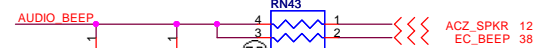
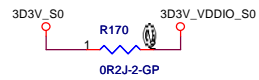
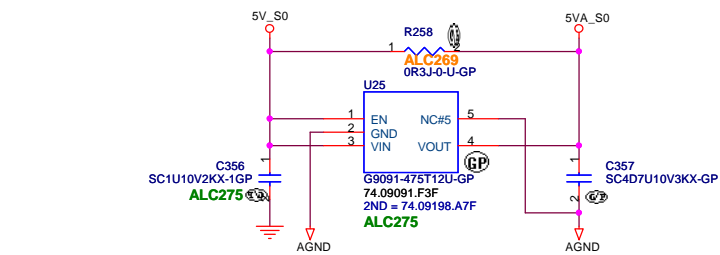
## LAN Connector



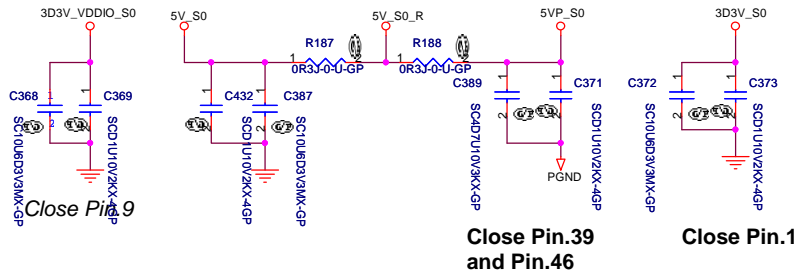
DVT 1ST

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

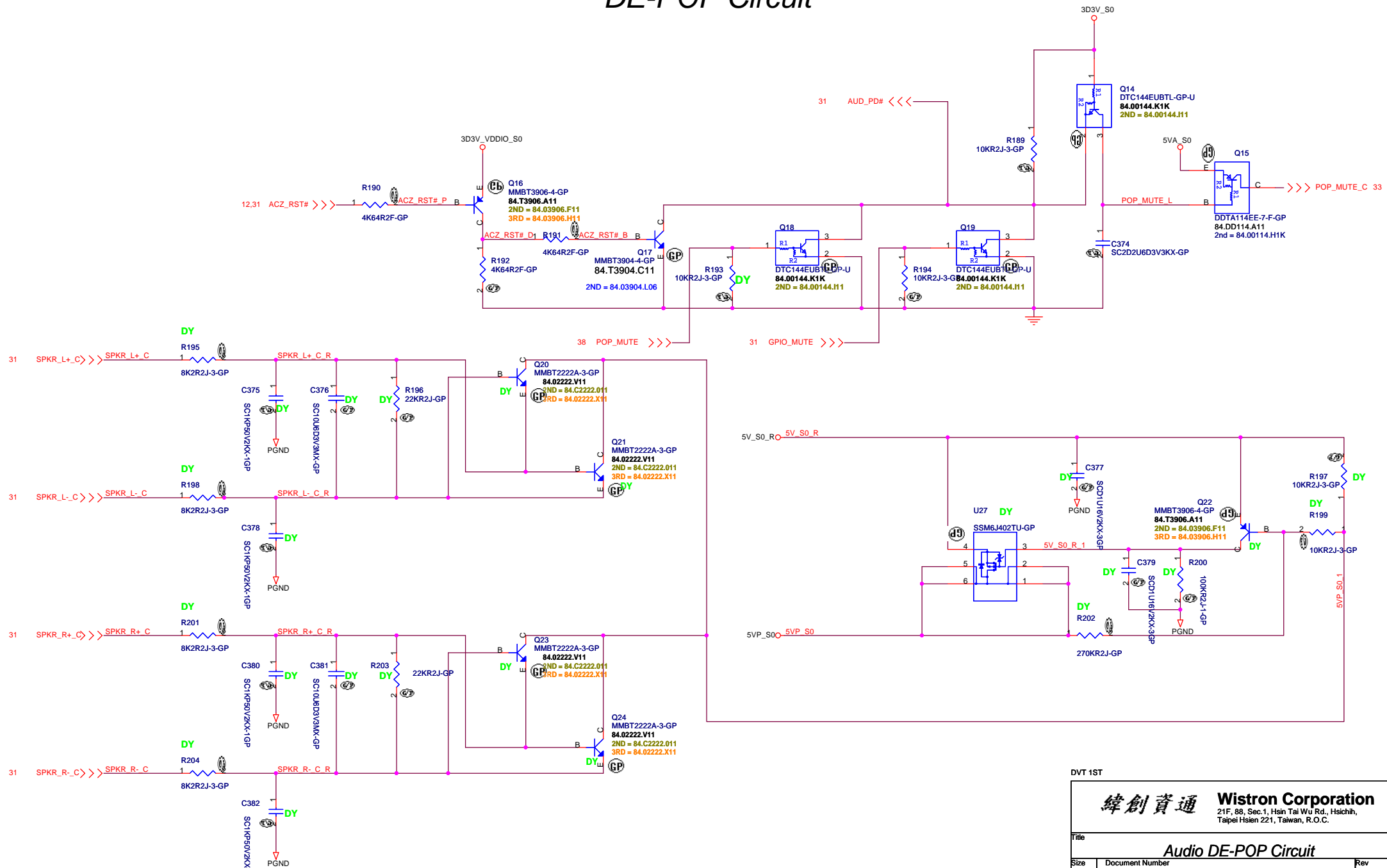
Title		
LAN CONN		
Size	Document Number	Rev
	TUCANA	SB
Date: Wednesday, July 07, 2010	Sheet 30 of 56	



1. BOTTOM CLOSE TO CODEC  
2, TOP CLOSE TO BTB CONNECTOR



## DE-POP Circuit



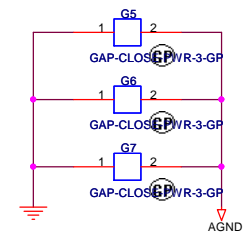
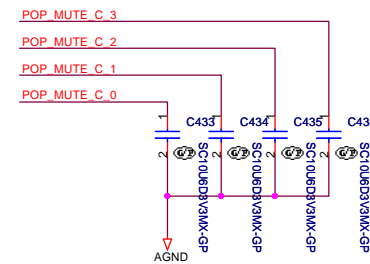
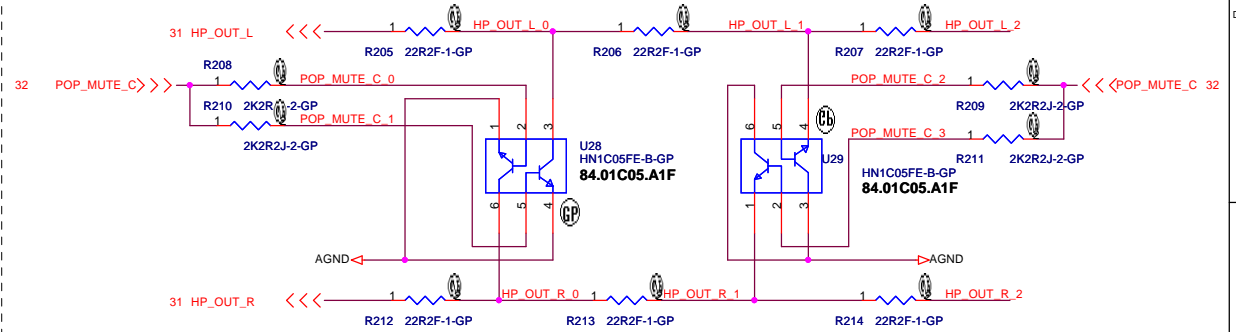
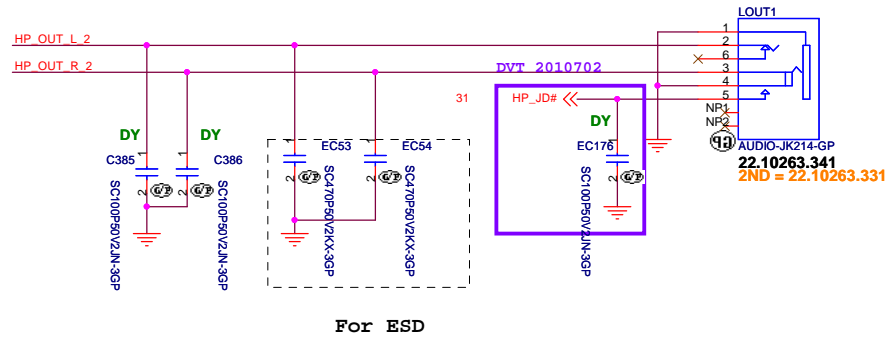
DVT 1ST

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Taipei Hsien 221, Taiwan, R.O.C.

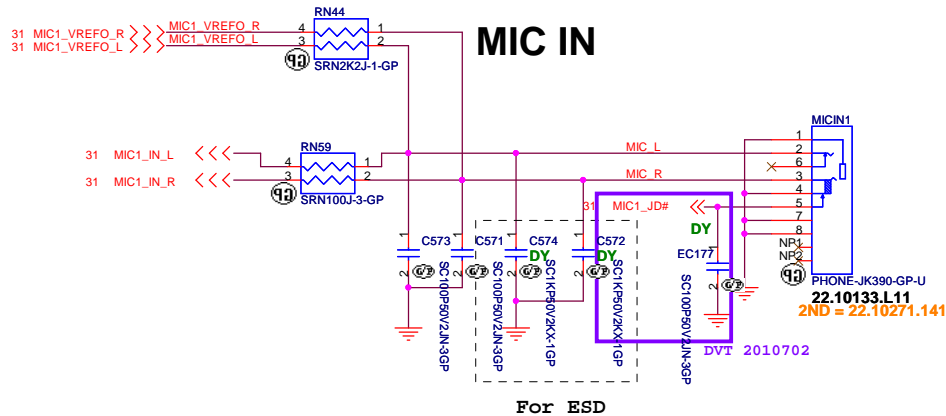
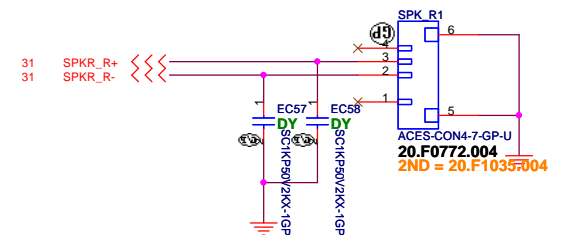
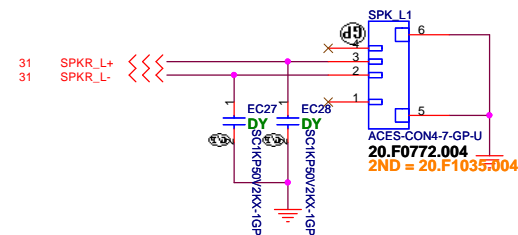
Title			
Audio DE-POP Circuit			
Size	Document Number		Rev
	TUCANA		SB
Date:	Wednesday, July 07, 2010	Sheet 32 of	56



## LINE OUT



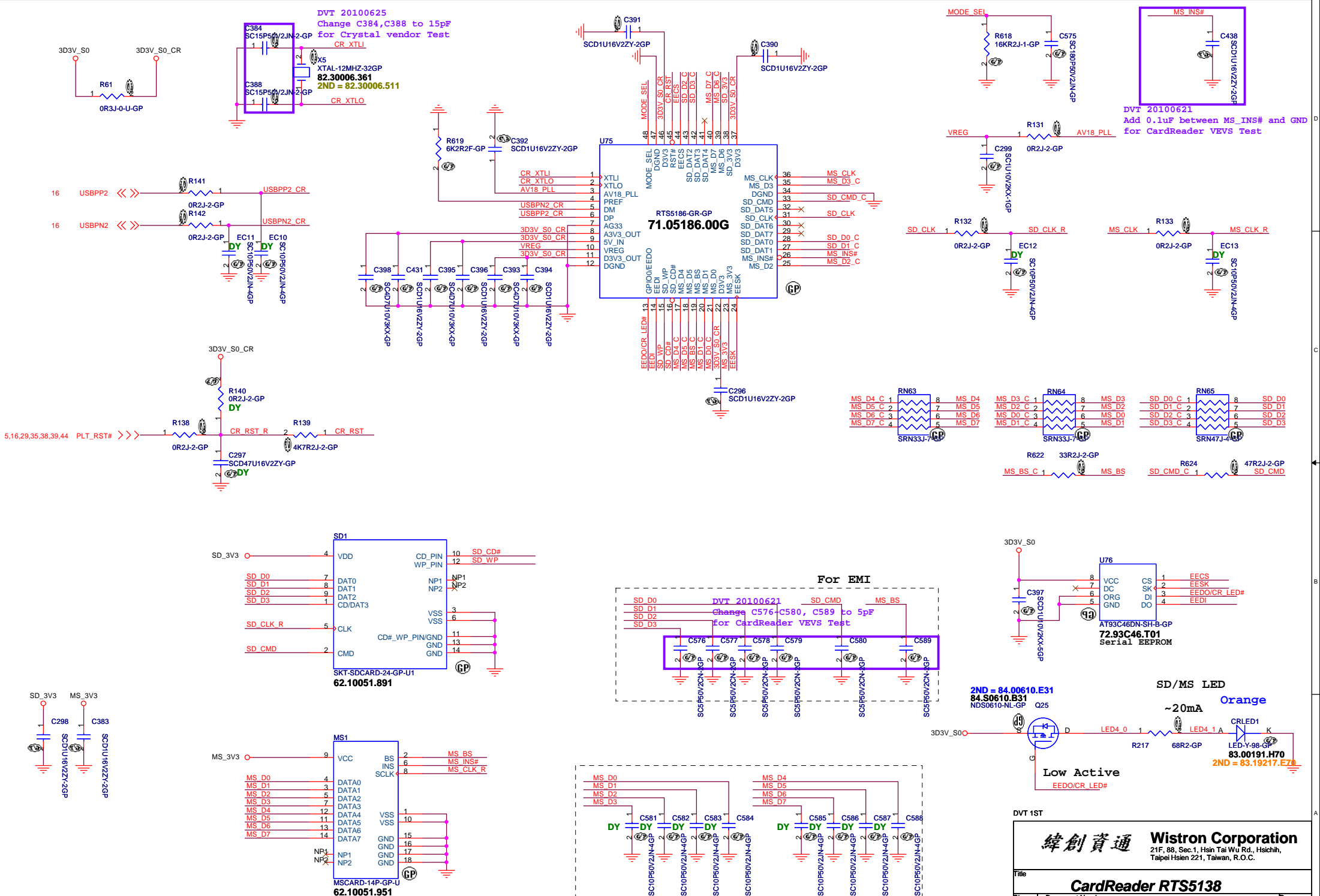
## Internal Speaker CONN



DVT 1ST

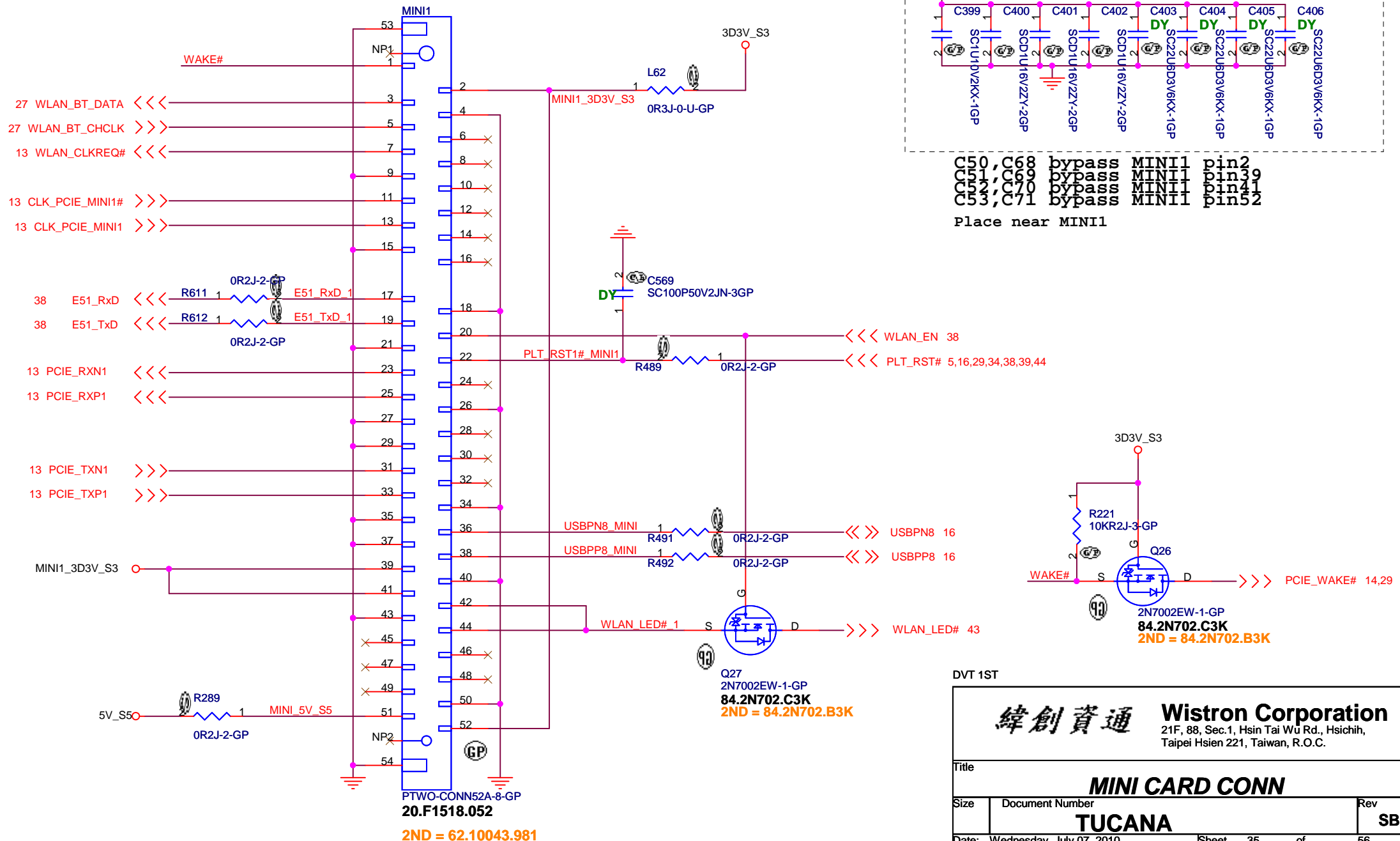
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Audio Jack & Speaker		
Size	Document Number	Rev
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# Mini Card Connector(WLAN)

WLAN\_EN:  
Low: disable the radio  
High: enable the radio



DVT 1ST

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Title

**MINI CARD CONN**

Size

Document Number

**TUCANA**

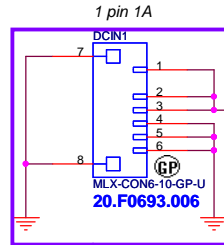
Rev

**SB**

Date: Wednesday, July 07, 2010

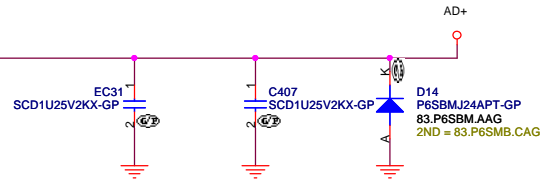
Sheet 35 of 56

## DC IN Connector



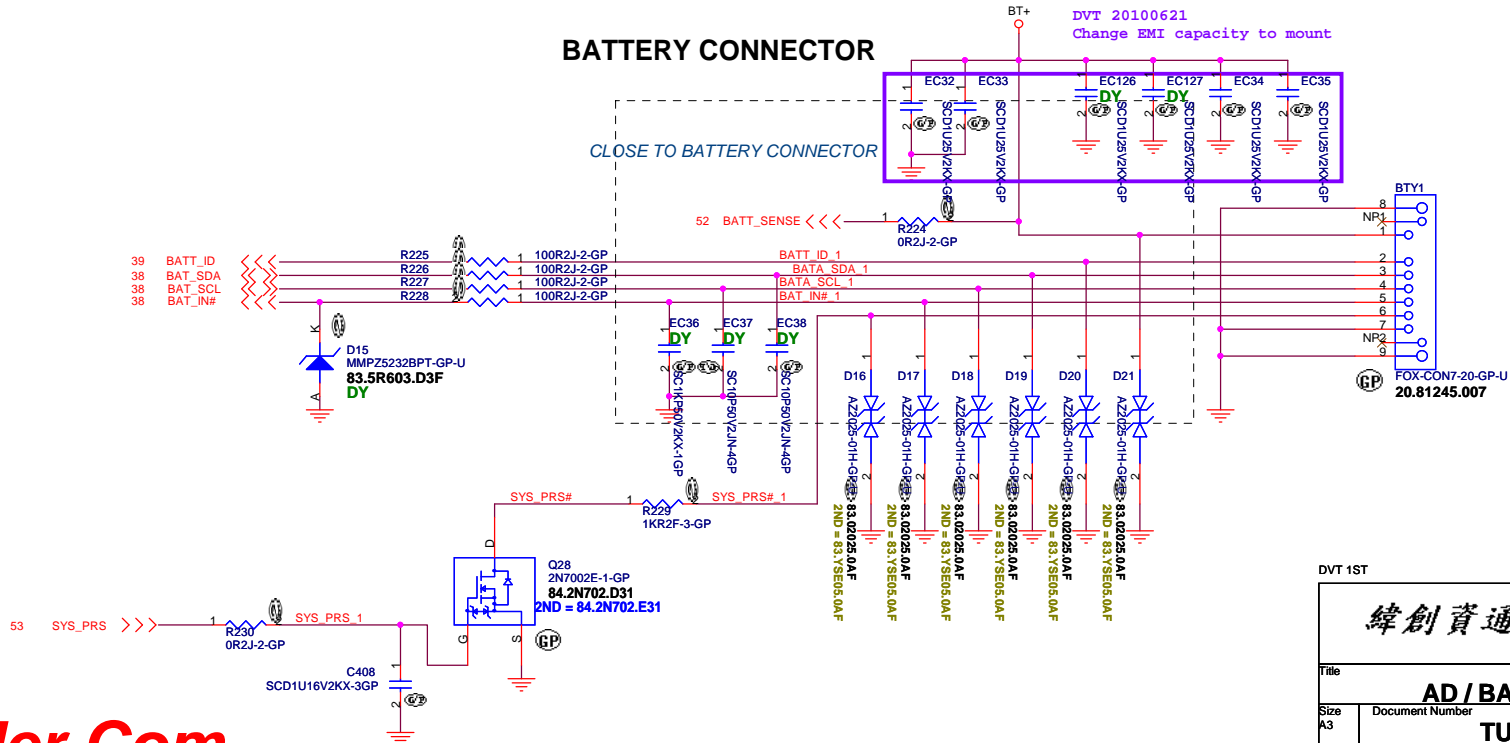
DVT 20100610  
Change DCIN1 to 20.F0693.006  
(follow connector list)

## Adaptor in to generate DCBATOUT



## BATTERY CONNECTOR

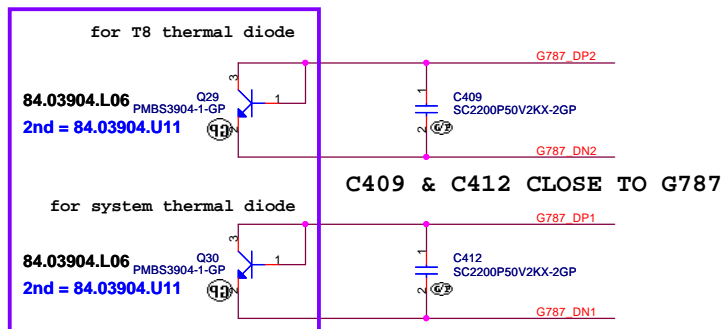
CLOSE TO BATTERY CONNECTOR



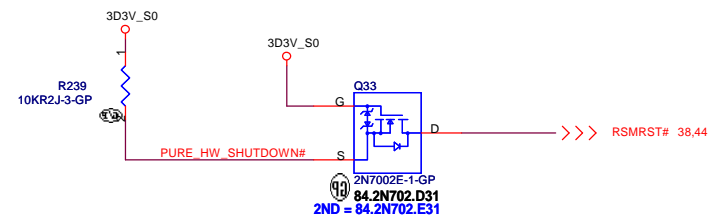
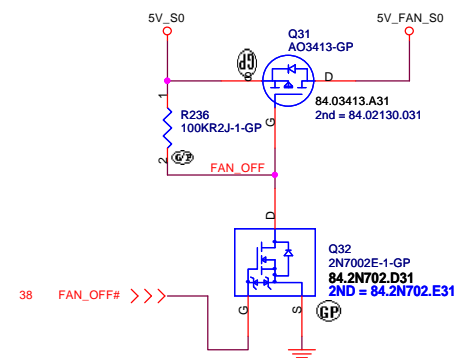
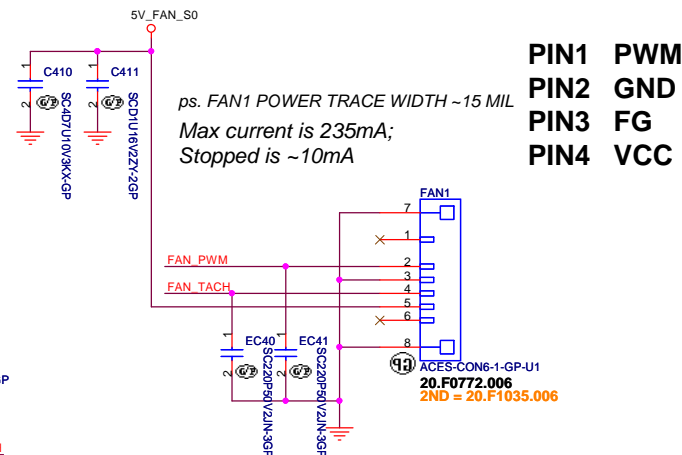
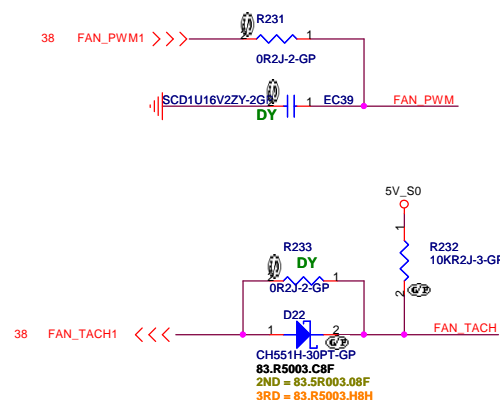
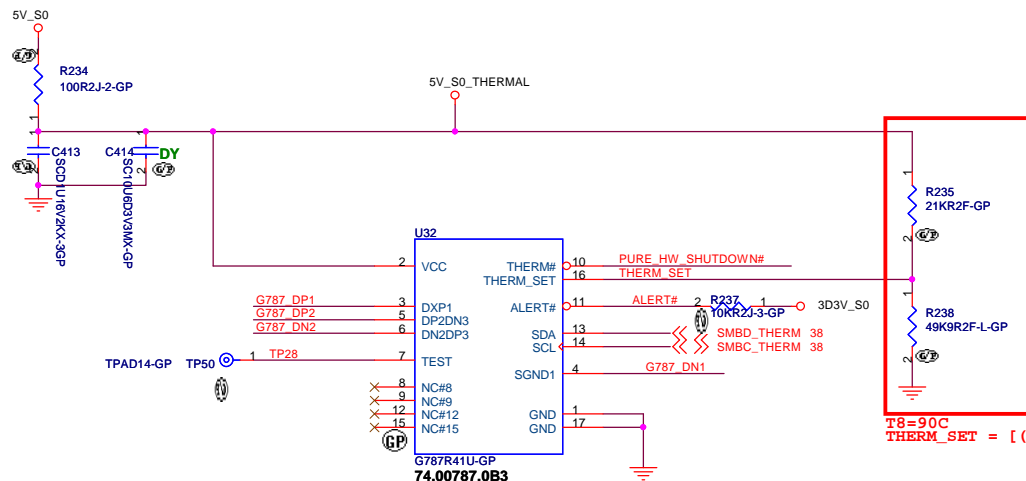
DVT 1ST

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
AD / BATT CONN		
Size	Document Number	Rev
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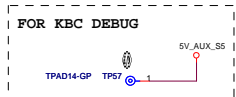
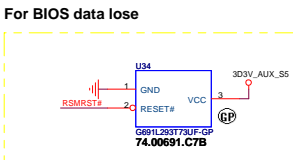
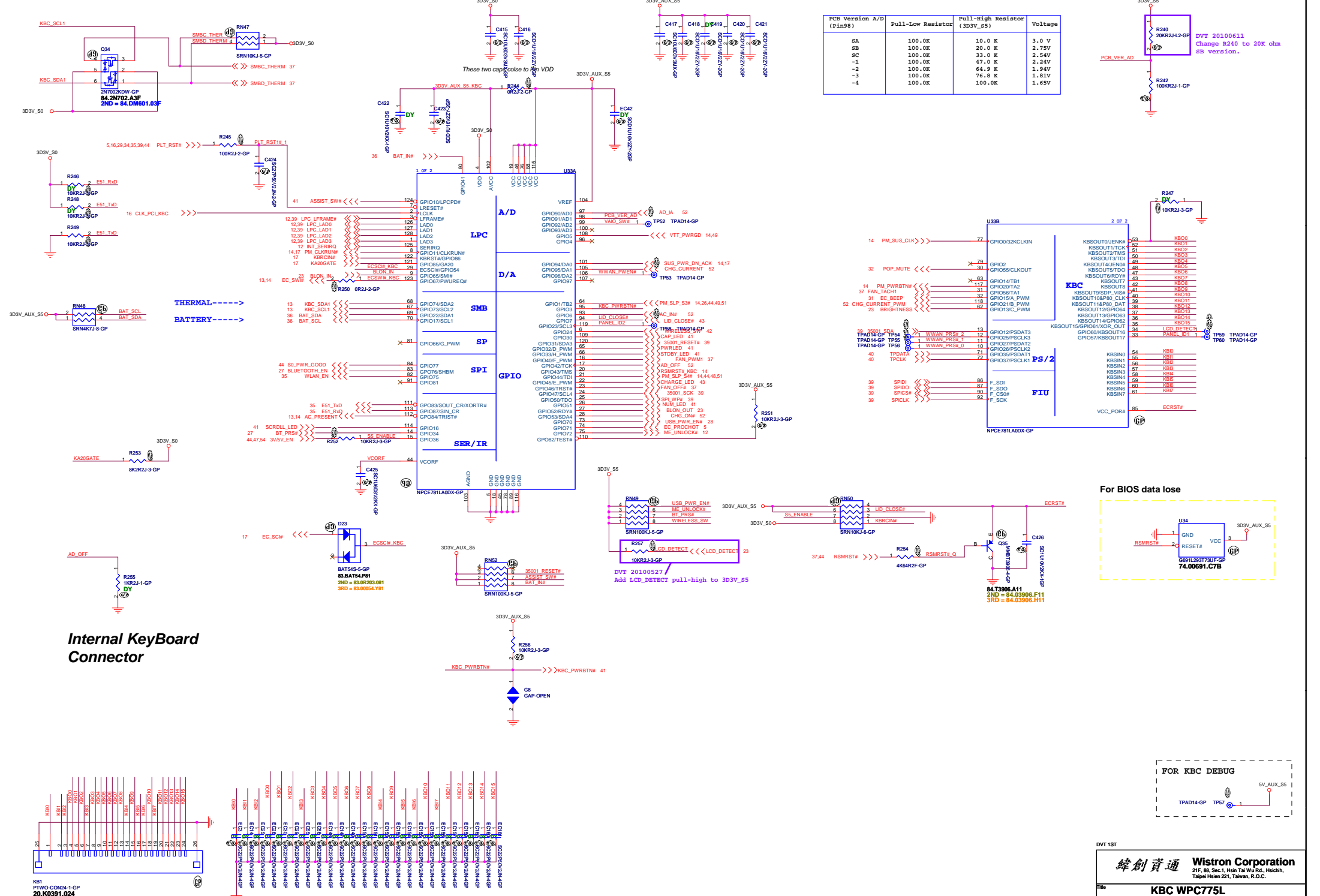
DVT 20100705  
Delete Q29,Q30 main source 84.T3904.C11, follow CARAVEL-CP design



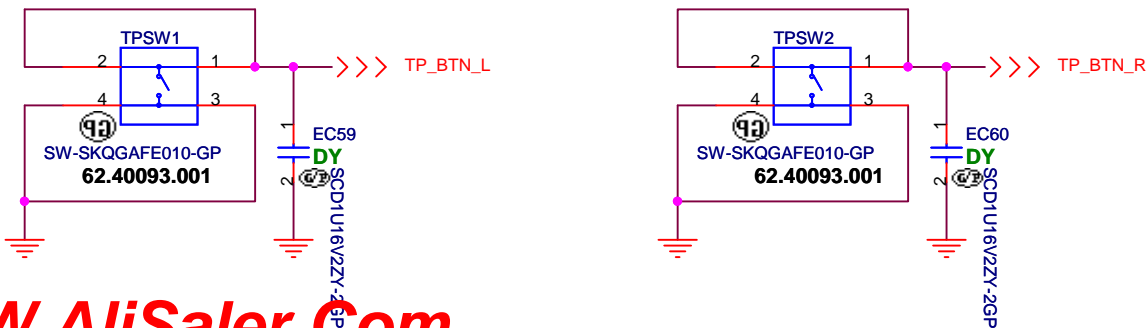
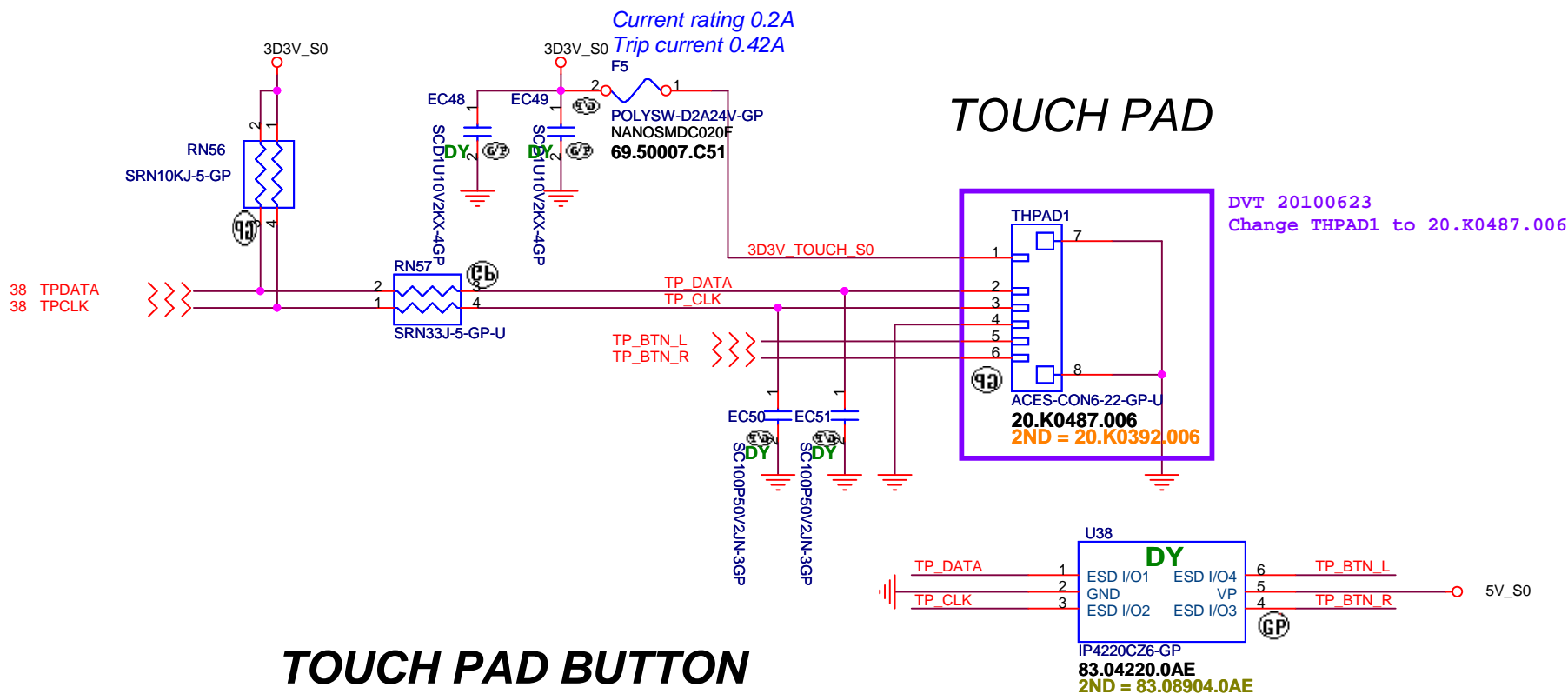
DVT 1ST

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title Thermal/Fan Controllor  
Size Document Number TUCANA  
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DVT 1ST

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**Wistron Corporation**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**TouchPad**

Size  
A4

Document Number

**TUCANA**

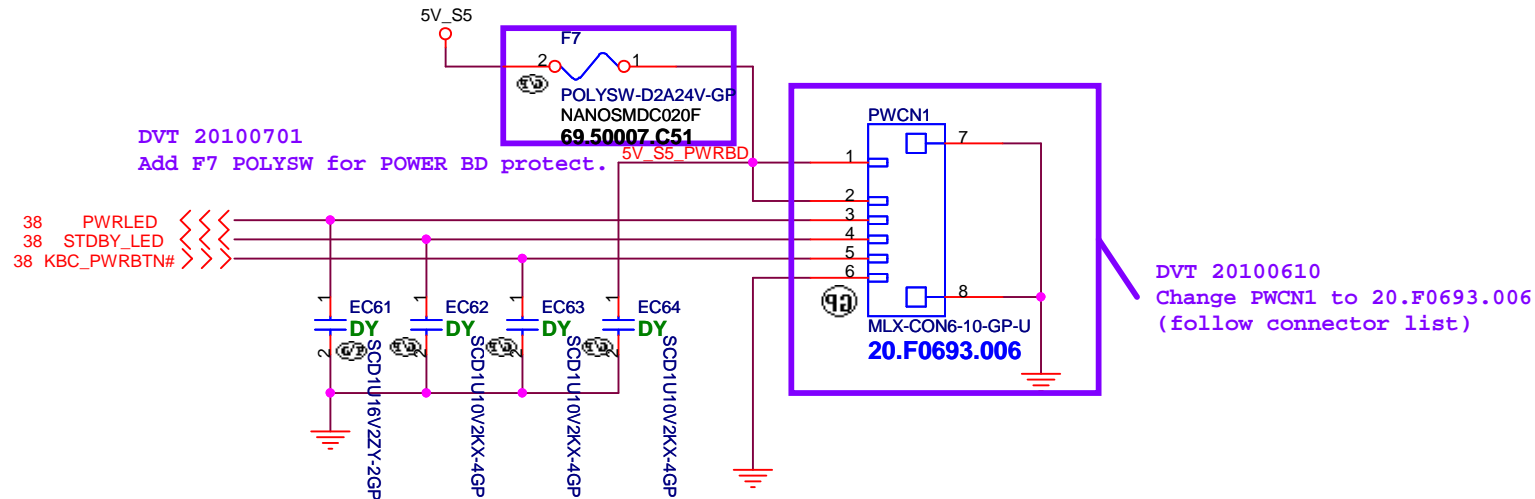
Rev  
**SB**

Date: Wednesday, July 07, 2010

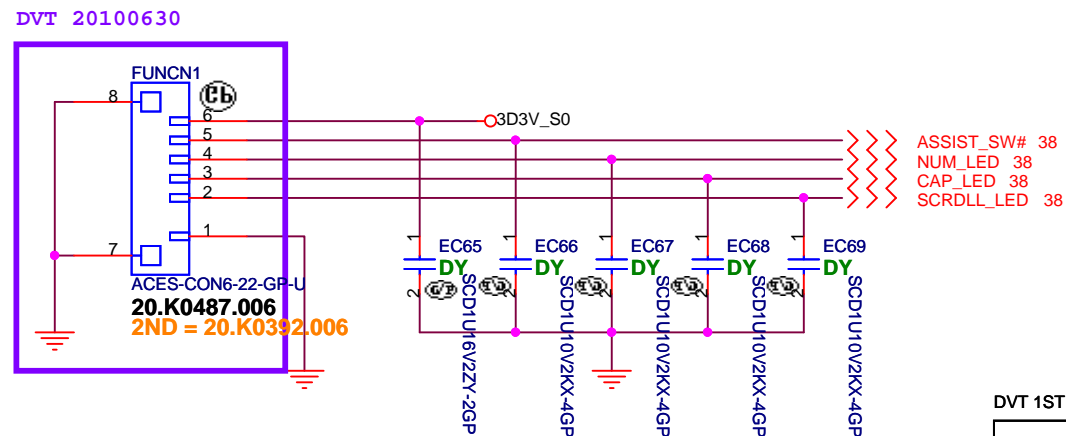
Sheet 40 of 56



# POWER BUTTON BD CONN



# FUNCTION BD CONN



DVT 1ST

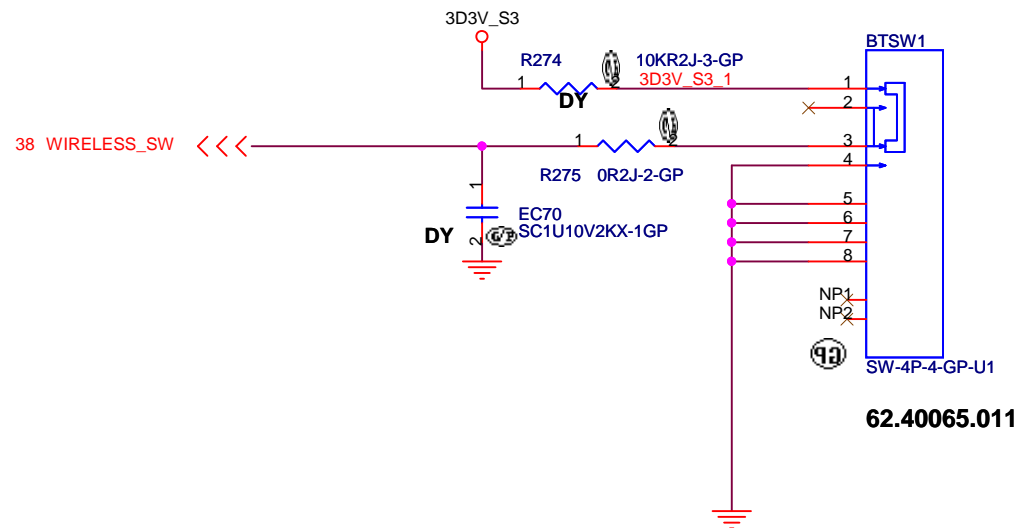
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title  
**FUNCTION BD & POWER BD**

Size Document Number  
**TUCANA**  
Rev  
**SB**

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# WLAN SWITCH



DVT 1ST

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Switch**

Size

Document Number

**TUCANA**

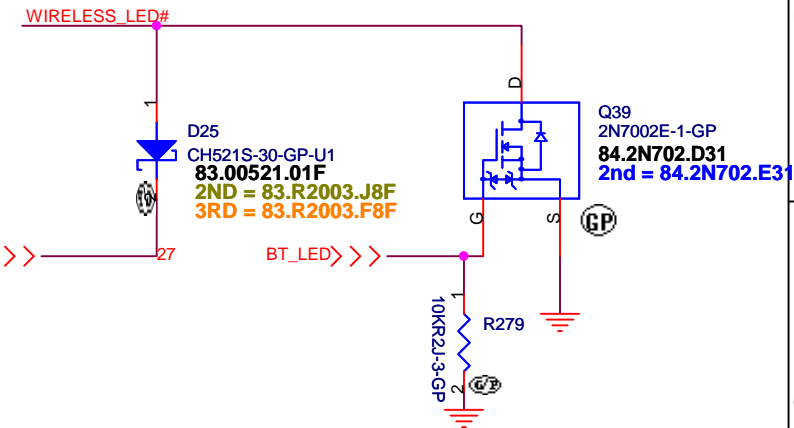
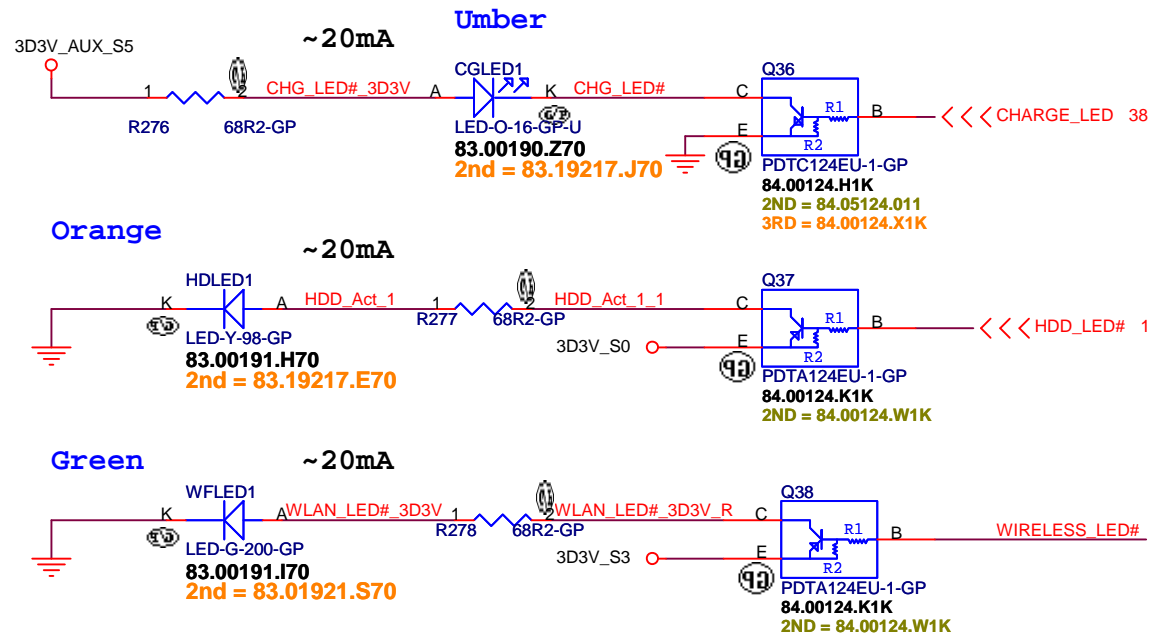
Rev

**SB**

Date: Wednesday, July 07, 2010

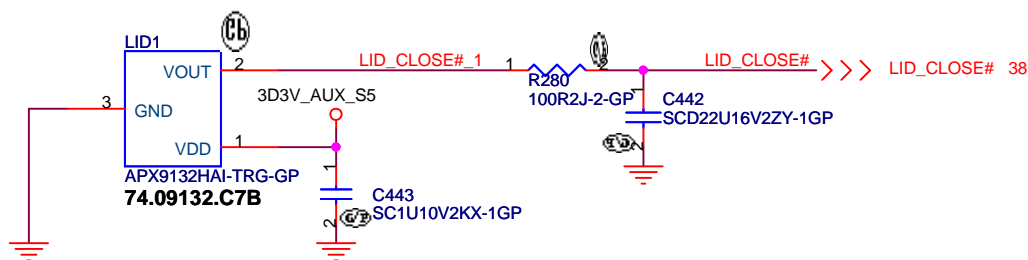
Sheet 42 of 56

# LED



active	High	Low
WWAN(W_DISABLE#)	ON	OFF
WLAN(WLAN_LED#)	OFF	ON
Bluetooth(BT_LED)	ON	OFF

## Cover Up Switch



Common wireless SW(mechanical)	ON							
WLAN SW(software)	ON	OFF	ON	OFF	ON	OFF	ON	OFF
WWAN SW(software)	ON	ON	OFF	OFF	ON	ON	OFF	OFF
Bluetooth SW(software)	ON	ON	ON	ON	OFF	OFF	OFF	OFF
LED	TURN ON							OFF

DVT 1ST

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Lid Switch & LED**

Size

Document Number

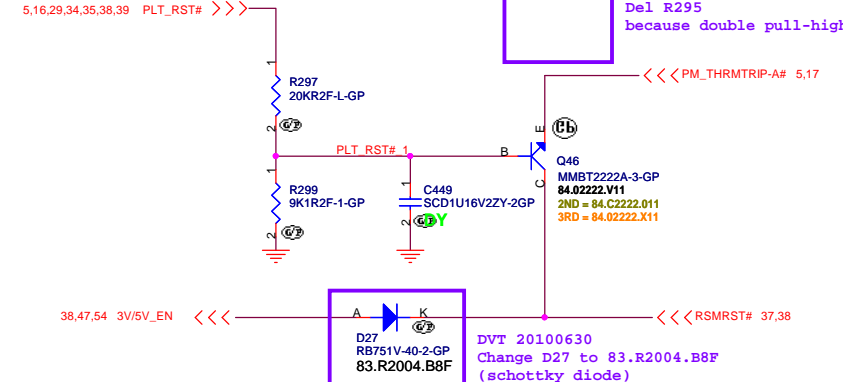
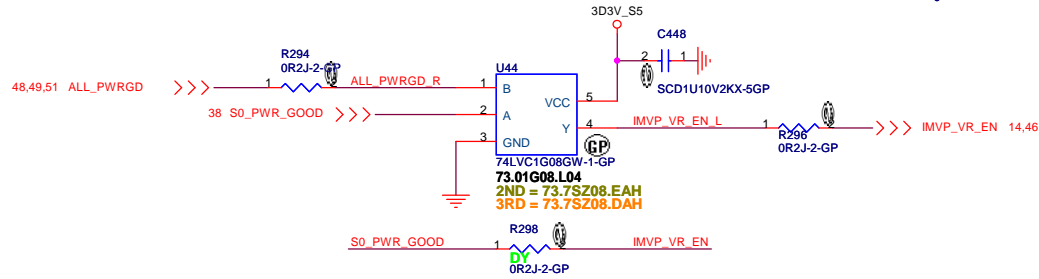
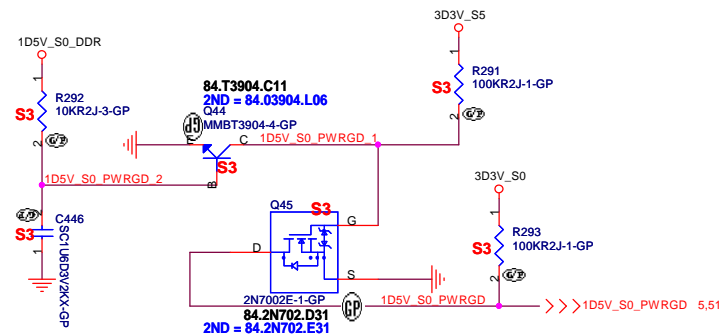
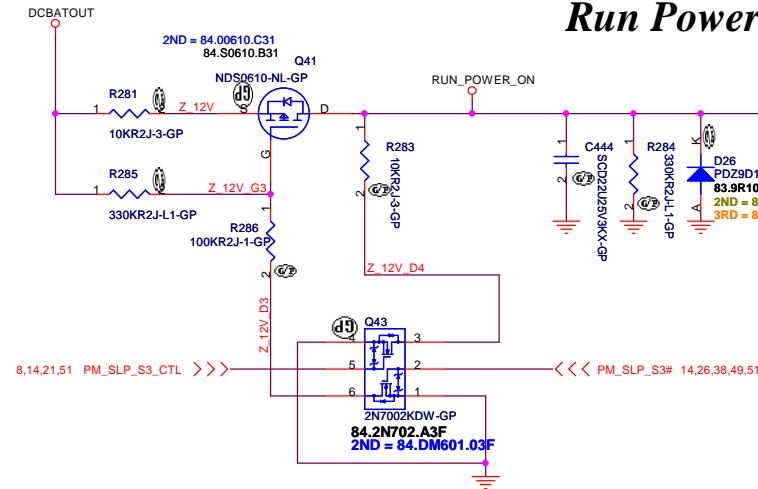
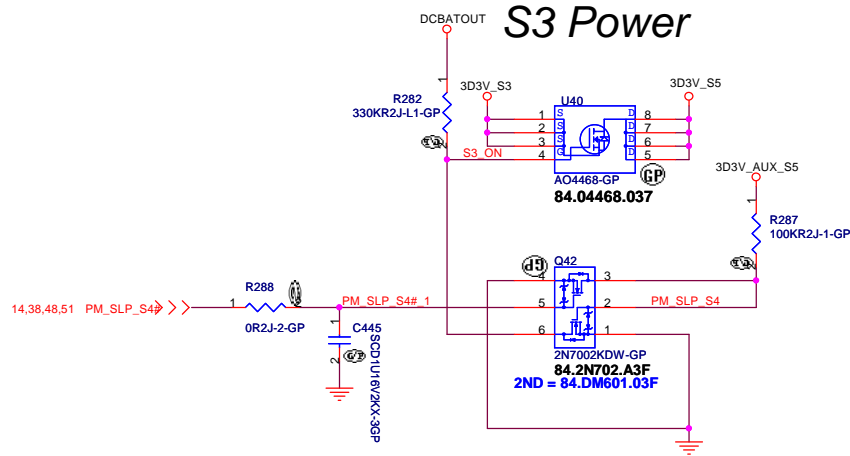
**TUCANA**

Rev

**SB**

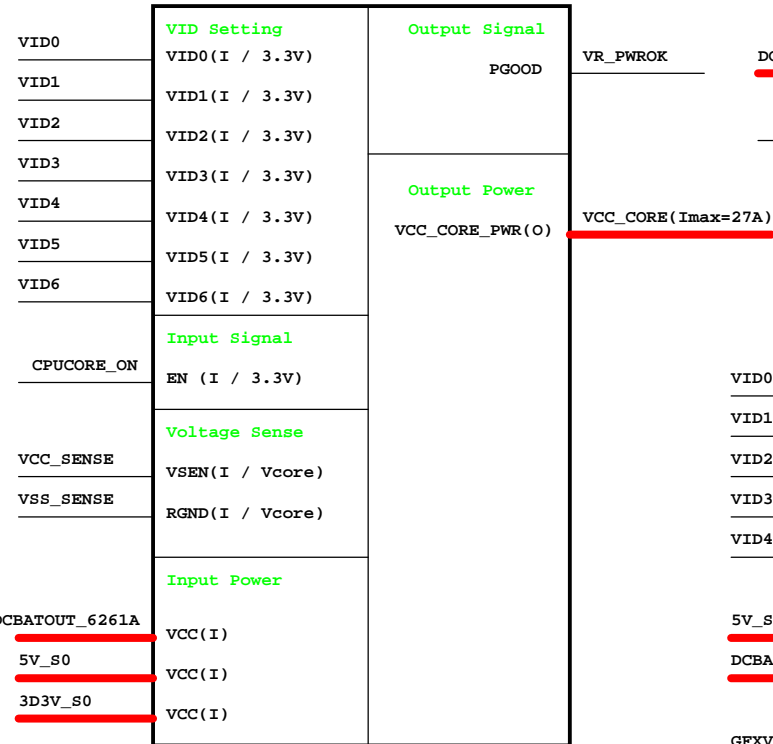
Date: Wednesday, July 07, 2010

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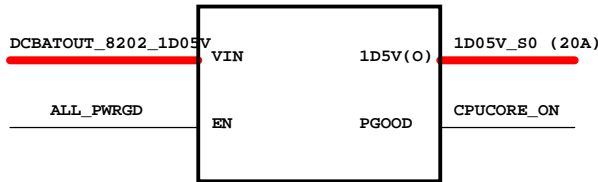


DVT 1ST			
<div> <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div> </div>			
Title RUN POWER			
Size	Document Number	Rev	
	TUCANA	SB	
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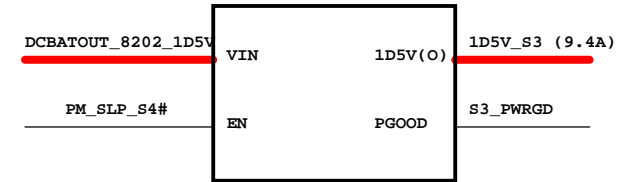
CPU\_CORE  
ADP3211



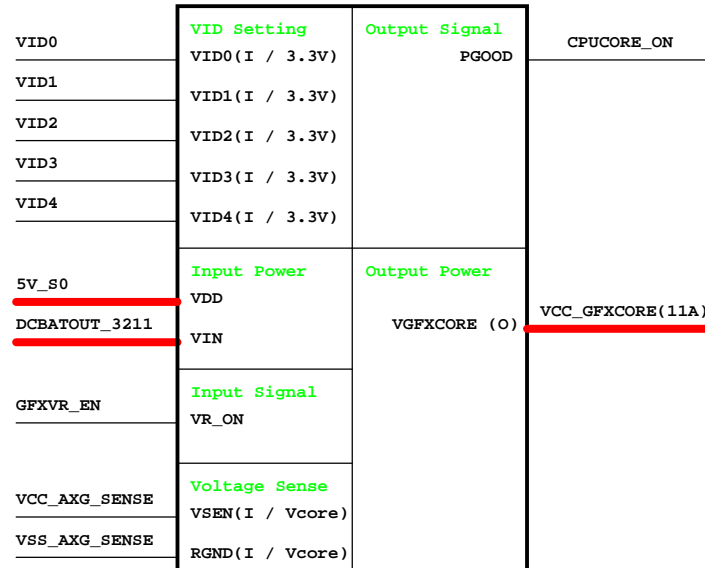
RT8209 1D05V\_S0



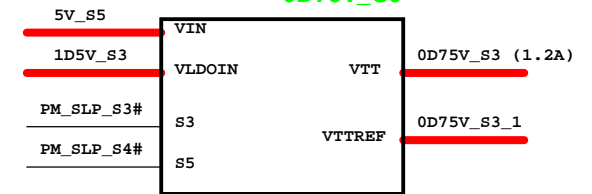
RT8209 1D5V\_S3



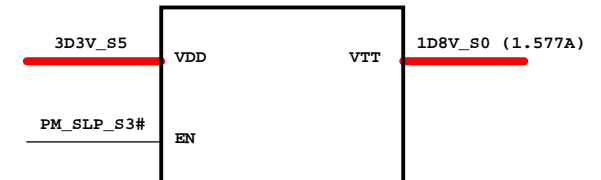
GFX\_CORE/ VGA\_CORE  
ADP3211



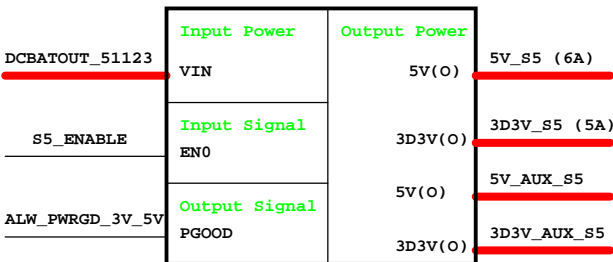
RT9026 0D75V\_S0



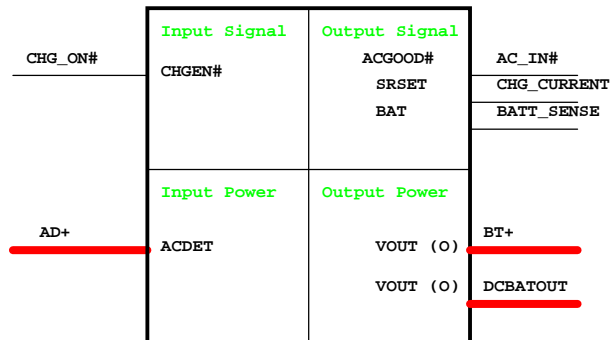
RT8015 1D8V\_S0



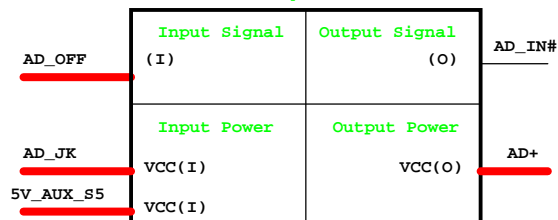
5V/3D3V  
RT8223



Charger BQ24751

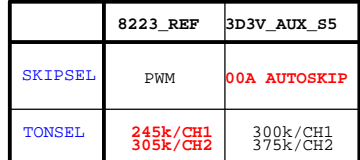
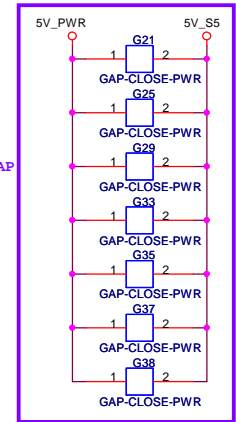


Adapter

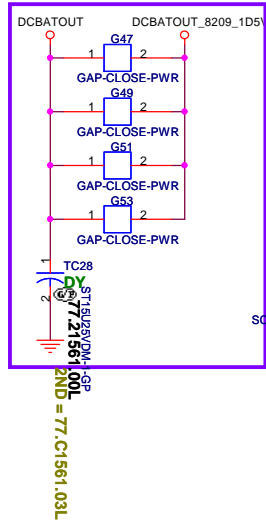


DVT 1ST

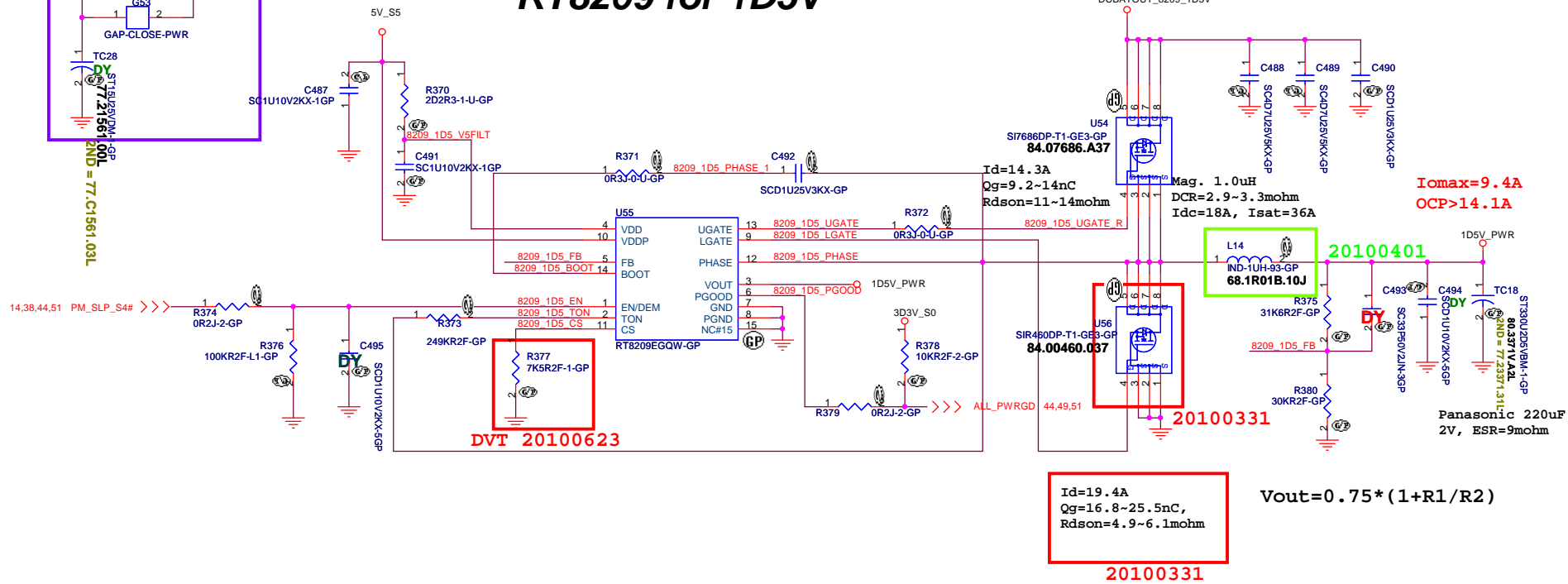




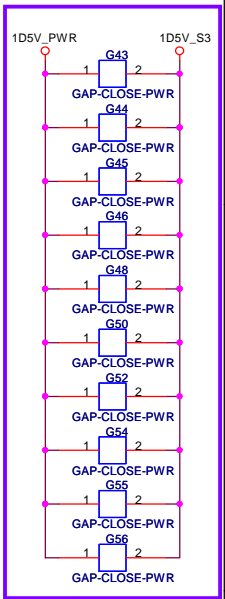
DVT 20100701  
Change OPEN-GAP to  
CLOSE-GAP



## RT8209 for 1D5V



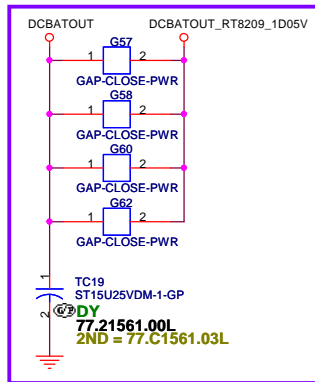
DVT 20100701  
Change OPEN-GAP to  
CLOSE-GAP



DVT 1ST

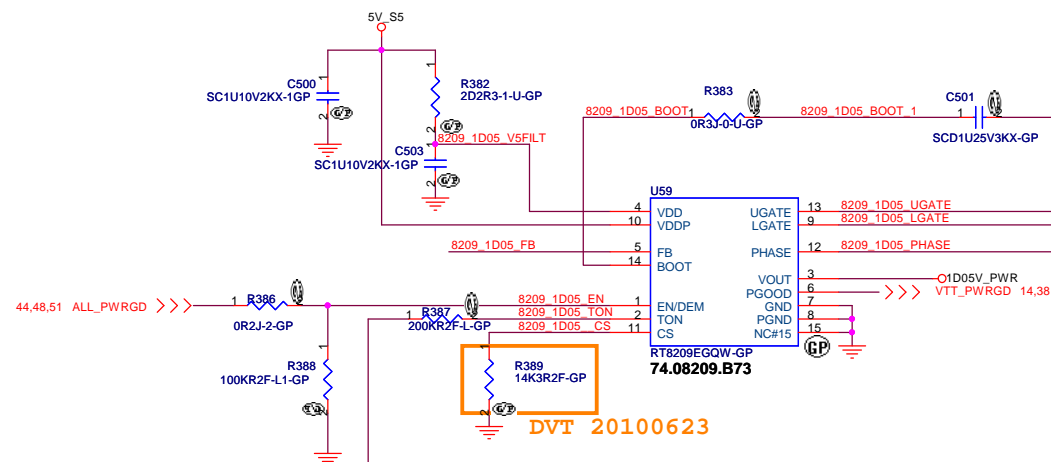
緯創資通 Wistron Corporation		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		RT8209 1D5V	
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DVT 20100701  
Change OPEN-GAP to  
CLOSE-GAP

## RT8209 1D05V



Id=24A  
Qg=11nC  
Rdson=9.4~13.5mohm

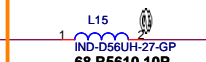
20100428



Id=50A  
Qg=46nC  
Rdson=2.3~3.6mohm

DVT 20100622

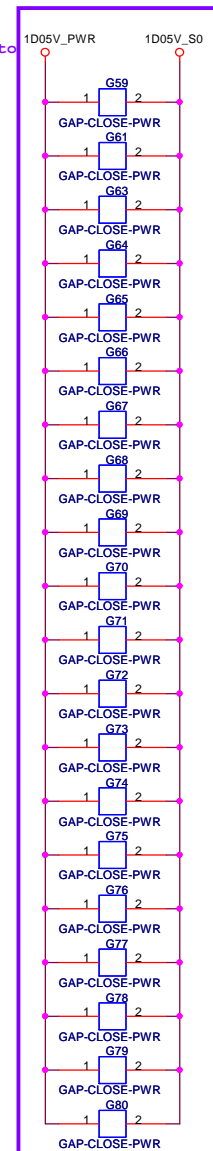
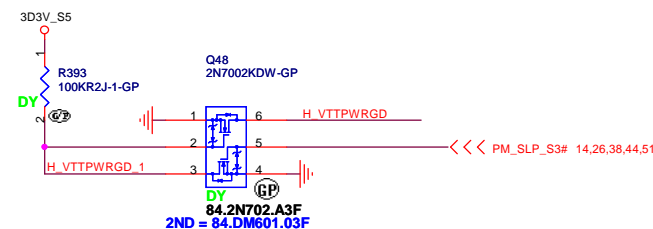
Mag. 0.56uH  
DCR=1.6~1.8mohm  
Idc=25A, Isat=40A



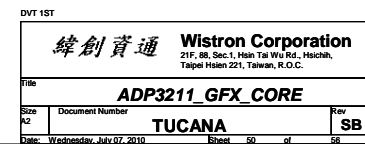
Iomax=20A  
OCP>30A

$$V_{out} = 0.75 * (1 + R1/R2)$$

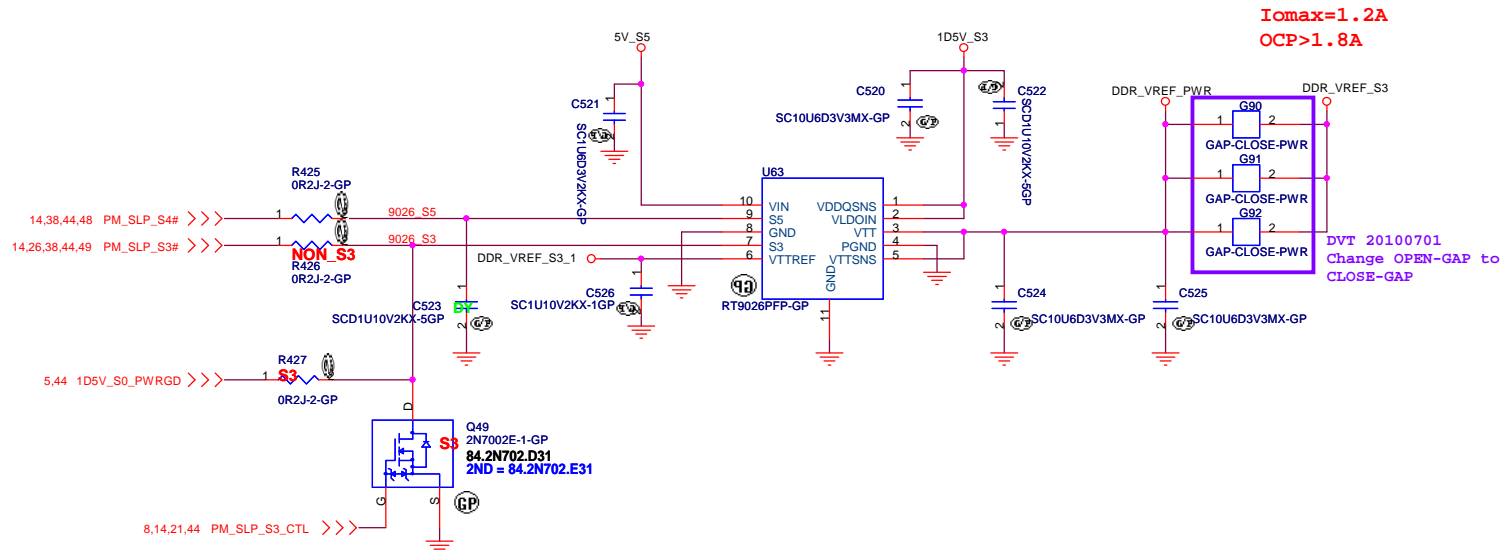
The processor needs to be warned about the VTT rails shutdown at least 100 ns before the VTT rail falls to -5% of nominal value.



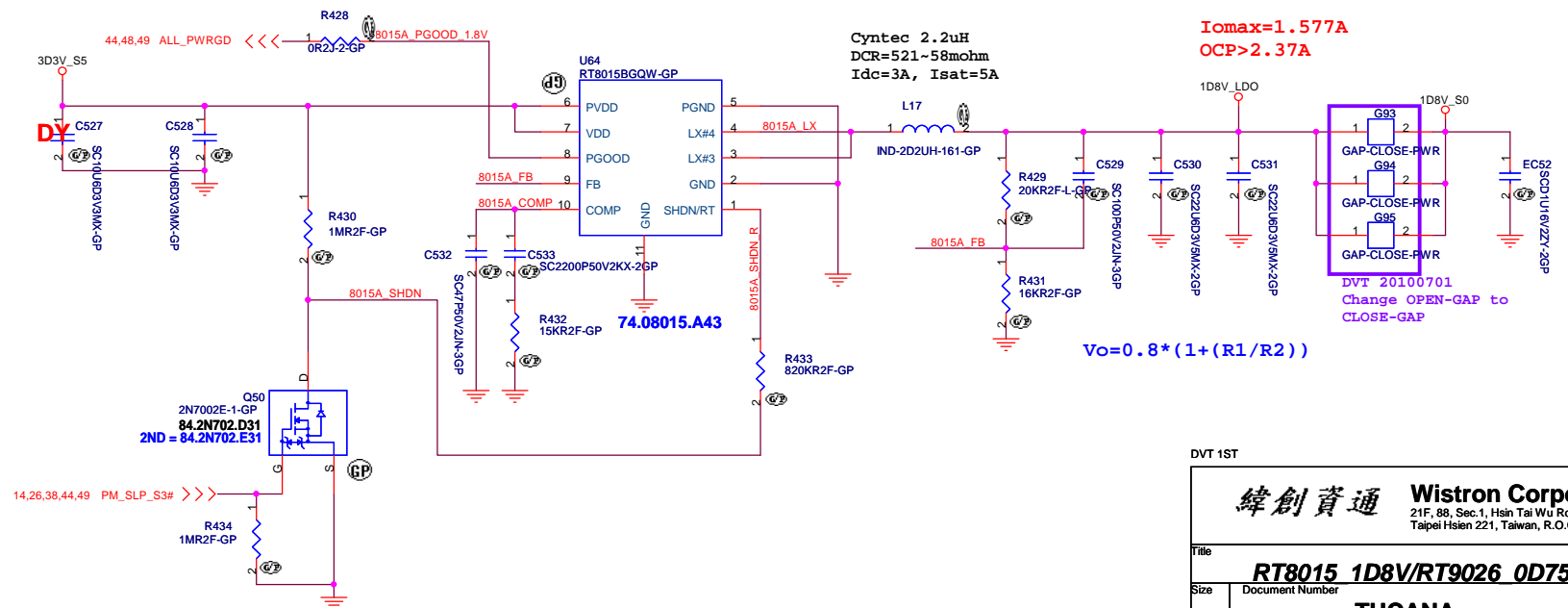
DVT 1ST



## RT9026 for 0D75V\_S3



## RT8015 for 1D8V\_S0

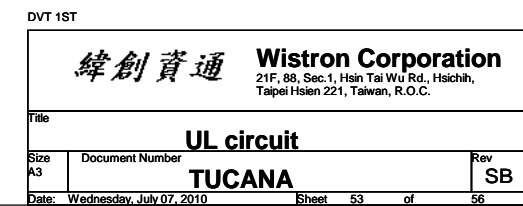
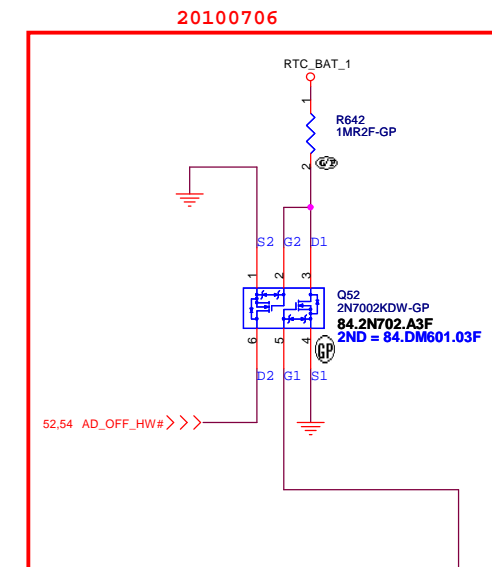


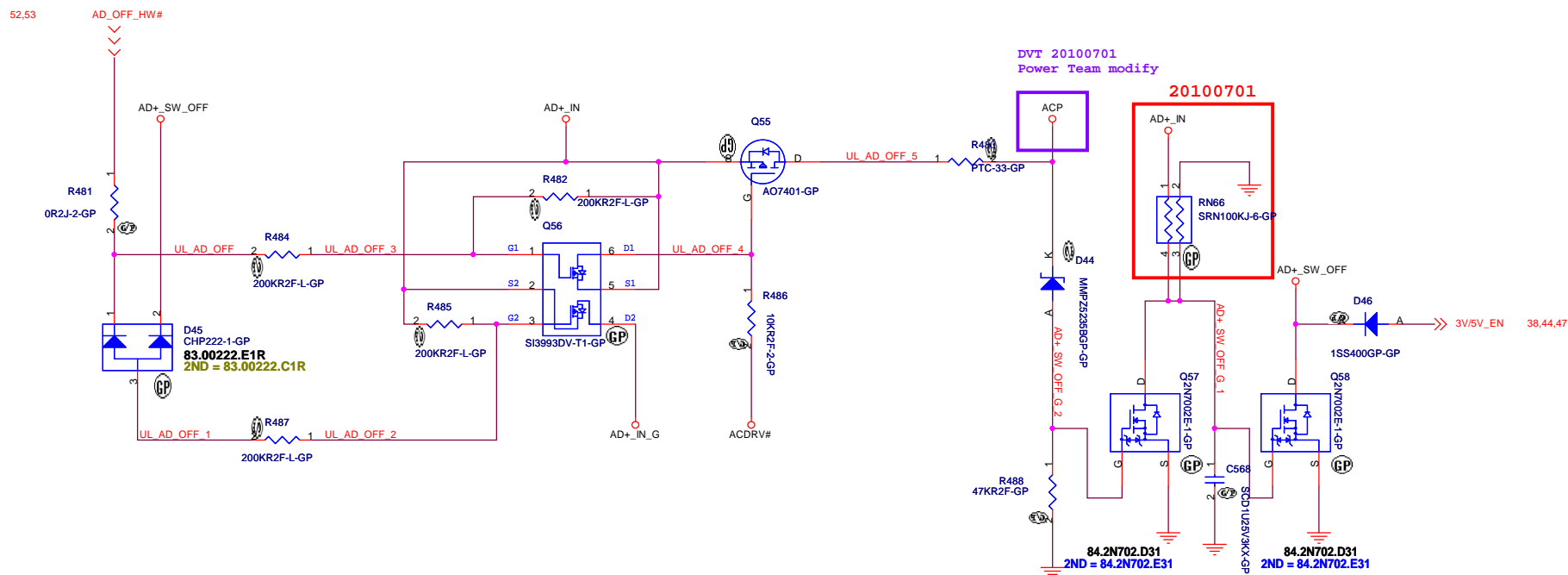
DVT 1ST

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>RT8015 1D8V/RT9026 0D75</b>			
Size	Document Number		Rev
	<b>TUCANA</b>		<b>SB</b>
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DVT 20100701  
Power Team modify

20100701

DVT 1ST

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Taipei Hsien 221, Taiwan, R.O.C.

Title			UVP Protect	
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EVT

2010/5/17	P.52[BQ24751_Charger]	Del D31 2nd 3rd source	2010/7/2	P.38[KBC_NPCE781L / KB]	Rename H_PROCHOT# to EC_PROCHOT
2010/5/17	P.25[HDMI CONN_PS8101]	Change 2nd source to 69.4R500.151		P.5[CPU SFF(2 of 8)-CLK/Thermal]	Add R128 for EC_PROCHOT pull-low to Gnd
2010/5/24	P.26[HDD Connector]	Change R148 to 3.3K ohm ,add C437 for PM_SLP_S3# Delay		P.5[CPU SFF(2 of 8)-CLK/Thermal]	Add Q61 for EC_PROCHOT to PROCHOT#
2010/5/27	P.38[KBC_NPCE781L / KB]	Add LCD_DETECT pull-high to 3D3V_S5		P.33[Audio Jack]	Add EC176 for HP_JD# to GND , Set Dummy for ESD.
2010/5/31	P.52[BQ24751_Charger]	Mount C546,R451,R449,Q51 for battery can't Changer			Add EC177 for MIC1_JD# to GND , Set Dummy for ESD.
2010/6/1	P.24[CRT CONN]	Change F6 to 69.44002.001, for Cadiz use		P.55[EMI/Spring/Boss]	Change SPR1 to 34.42T14.002
	P.33[Audio Jack]	Change MICIN1 to 20.10133.L11 , follow connector list			
	P.28[USB]	Change USB1,USB2,USB3 connector to 22.1032.1.Q71 [follow ME connector list]	2010/7/5	P.14[PCH (3 of 9)-DMI/FDI]	Change D3 to schottky diode.
2010/6/10	P.36[AD / BATT CONN]	Change DCIN1 to 20.F0693.006 (follow connector list)		P.37[Thermal / Fan Controllor]	Delete Q29,Q30 main source 84.T3904.C11, follow CARAVEL-CP design
	P.41[FUNCTION BD & POWER BD]	Change PWCN1 to 20.F0693.006 (follow connector list)	2010/7/6	P.53[UL CIRCUIT]	Rename R642 Pin1 contact to RTC_BAT_1 (Old use RTC_BAT),follow CARAVEL-CP
2010/6/11	P.41[FUNCTION BD & POWER BD]	Del FUNCN2 connector by ME request			
	P.38[KBC_NPCE781L / KB]	Change R240 to 20K ohm SB version.			
	P.25[HDMI CONN_PS8101]	Change R614--R617 to 200R2J , Set mount. [for EMI request]			
	P.25[HDMI CONN_PS8101]	Change C283,C364 to 1uF [for EMI request]			
	P.25[HDMI CONN_PS8101]	Change C282,C285 to 1KpF [for EMI request]			
2010/6/21	P.16[PCH (5 of 9)-PCI/USB]	Add PCL_REQ2# Pull-High to 3D3V_S0 by hang-up issue			
	P.31[Audio Codec ALC269]	Change EC23,EC24 to mount [for EMI request]			
	P.55[EMI/Spring/Boss]	Change DCBATOUT capacity to mount (EC71--83,EC89,EC90,EC124,EC164--169) [for EMI request]			
		Change 5V_S0 capacity to mount (EC173--EC175) [for EMI request]			
		Change 3D3V_S0 capacity to mount (EC91--94,EC104) [for EMI request]			
		Change 3D3V_S3 capacity to mount (EC84--87) [for EMI request]			
		Change VCC_GFXCORE capacity to mount (EC142--146) [for EMI request]			
		Change VCC_CORE capacity to mount (EC136--139) [for EMI request]			
	P.36[AD / BATT CONN]	Change BT+ capacity to mount (EC32--35) [for EMI request]			
	P.23[LCD CONN]	Change C258 to 470pF (BRIGHTNESS_CN) [for EMI request]			
	P.34[CardReader RTS5186]	Add C272 between BLON_OUT_R and Gnd [for EMI request]			
		Change C576--580,C589 to 5pF [CardReader VEVs test]			
	P.24[CRT CONN]	Add 0.1uF between MS_INS# and GND [CardReader VEVs test]			
		Change R114,R115,R119,R120 to 2.7K ohm [CRT VEVs report]			
2010/6/22	P.53[UL CIRCUIT]	UL Circuit modify. [Prevent the RTC_BAT keep protecting.]			
2010/6/23	P.40[TouchPad]	Change THPAD1 to 20.K0487.006 [Follow ME connector list]			
	P.55[EMI/Spring/Boss]	Change SPR3 to DY [for EMI request]			
	P.53[UL CIRCUIT]	Add D42(83.00400.D1F), D41(83.00400.D1F) components. [Reduce the RTC_BAT discharge]			
		connect R467 pin1 to D41 and D42 pin k. [Reduce the RTC_BAT discharge]			
		connect D42 pin A to AD+_in. [Reduce the RTC_BAT discharge]			
	P.46[ADP3211_CPU CORE]	connect D41 pin A to ACP_UVP [Reduce the RTC_BAT discharge]			
		Change U45 to 84.08030.037 [Improve High side Vgs induce voltage]			
		Change U47 to 84.08028.037 [Improve High side Vgs induce voltage]			
		Change U48 to 84.08028.037 [Improve High side Vgs induce voltage]			
		add these statements. [follow Power Team design]			
	P.47[RT8223_5V/3D3V]	Change R316 to 7.87K ohm (old use 7.32K ohm) [Tune CPU Imon value]			
		Change C465 to 680pF (old use 560pF) [Tune CPU load line value]			
		Change R353 to 84.5K ohm (old use 97.6K ohm) [Adjust OCP value]			
	P.48[RT8209_1D5V]	Change L13 to 2.2uH (old use 3.3uH) [IC needs higher sensing voltage to detect it.]			
	P.49[RT8209_1D05V]	Change R377 to 7.5K ohm (old use 11.5K ohm) [Adjust OCP value]			
		Change R389 to 14.3K ohm (old use 10.2K ohm) [Adjust OCP value]			
	P.50[ADP3211_GFX_CORE]	Change L15 to 0.56uH (old use 0.45uH) [Reduce the output ripple voltage]			
		Change R419 to 56.2K ohm (old use 53.6K ohm) [Tune GFX load line value]			
		Change TC26 to mount.(old Dummy) [Improve under-shoot voltage phenomenon]			
2010/6/25	P.13[PCH (2 of 9)-PCIE/CLK/SMB]	Change C156,C157 to 12pF [for Crystal vendor Test]			
	P.29[LAN AR8131M]	Change C346 to 18pF [for Crystal vendor Test]			
	P.34[CardReader RTS5186]	Change C384,C388 to 15pF [for Crystal vendor Test]			
2010/6/29	P.17[PCH (6 of 9)-GPIO/RSVD]	Change RN31 to R648,R649 (56 ohm) for pull-high 1.05V_S0			
		Del R295 , because double pull-high			
2010/6/30	P.41[FUNCTION BD & POWER BD]	Change pin define of the FUNCN1 connector [follow the way of FFC folder for ME]			
	P.19[PCH (8 of 9)-PWR\SATA\USB]	Del R101 , only use 3D3V_S5			
	P.12[PCH (1 of 9)-SATA/RTC/HDA]	Change D1 to 83.R2003.I81 (SCHOTTKY DIODE)			
	P.25[HDMI CONN_PS8101]	Change Q12 to 84.2N702.D31 (ESD Protected 1.0KV)			
	P.44[RUN POWER]	Change D27 to 83.R2004.B8F (schottky diode)			
2010/7/1	P.46[ADP3211_CPU CORE]	Change OPEN-GAP to CLOSE-GAP (G9--14)			
	P.47[RT8223_5V/3D3V]	Change OPEN-GAP to CLOSE-GAP (G18,G22,G26,G30,G20,G24,G28,G32)			
		Change OPEN-GAP to CLOSE-GAP (G19,G23,G27,G31,G34,G36)			
	P.48[RT8209_1D5V]	Change OPEN-GAP to CLOSE-GAP (G21,G25,G29,G33,G35,G37,G38)			
		Change OPEN-GAP to CLOSE-GAP (G47,G49,G51,G53)			
	P.49[RT8209_1D05V]	Change OPEN-GAP to CLOSE-GAP (G43--46,G48,G50,G52,G54--56)			
		Change OPEN-GAP to CLOSE-GAP (G57,G58,G60,G62)			
	P.50[ADP3211_GFX_CORE]	Change OPEN-GAP to CLOSE-GAP (G59,G61,G63--80)			
	P.51[RT8015_1D8V/ RT9026_0D75]	Change OPEN-GAP to CLOSE-GAP (G81--86)			
	P.41[FUNCTION BD & POWER BD]	Change OPEN-GAP to CLOSE-GAP (G90--95)			
	P.54[UVP Protect]	Add F7 POLYSW for POWER BD 5V_S5 protect.			
		Delete R483 and add RN66. (RN66 part number is 66.10436.04L)			
		Connect AD+_IN to RN66 pin 1.			
		Connect RN66 pin2 to GND.			
	P.53[UL CIRCUIT]	Connect RN66 pin3 and pin4 to AD+_SW_OFF_G_1			
		Change R468 part number to the 64.36025.6DL			
		Change R469 to the part number 64.30025.6DL			
		Cummy R471 and mount D39.			
		Delete D40 and RN58.			
		Add R642. (Part number is 64.10045.6DL )			
		Connect R642 pin 1 to RTC_BAT.			
		Connect R642 pin2 to Q52 pin 2 and pin3.			
		Connect ACP to R435 pin 1.			
	P.52[BQ24751_Charger]	UPDATE BTCN1 PCB LAYOUT (REMOVE THE NPTH)			
	P.27[Bluetooth]				

<Core Design>

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